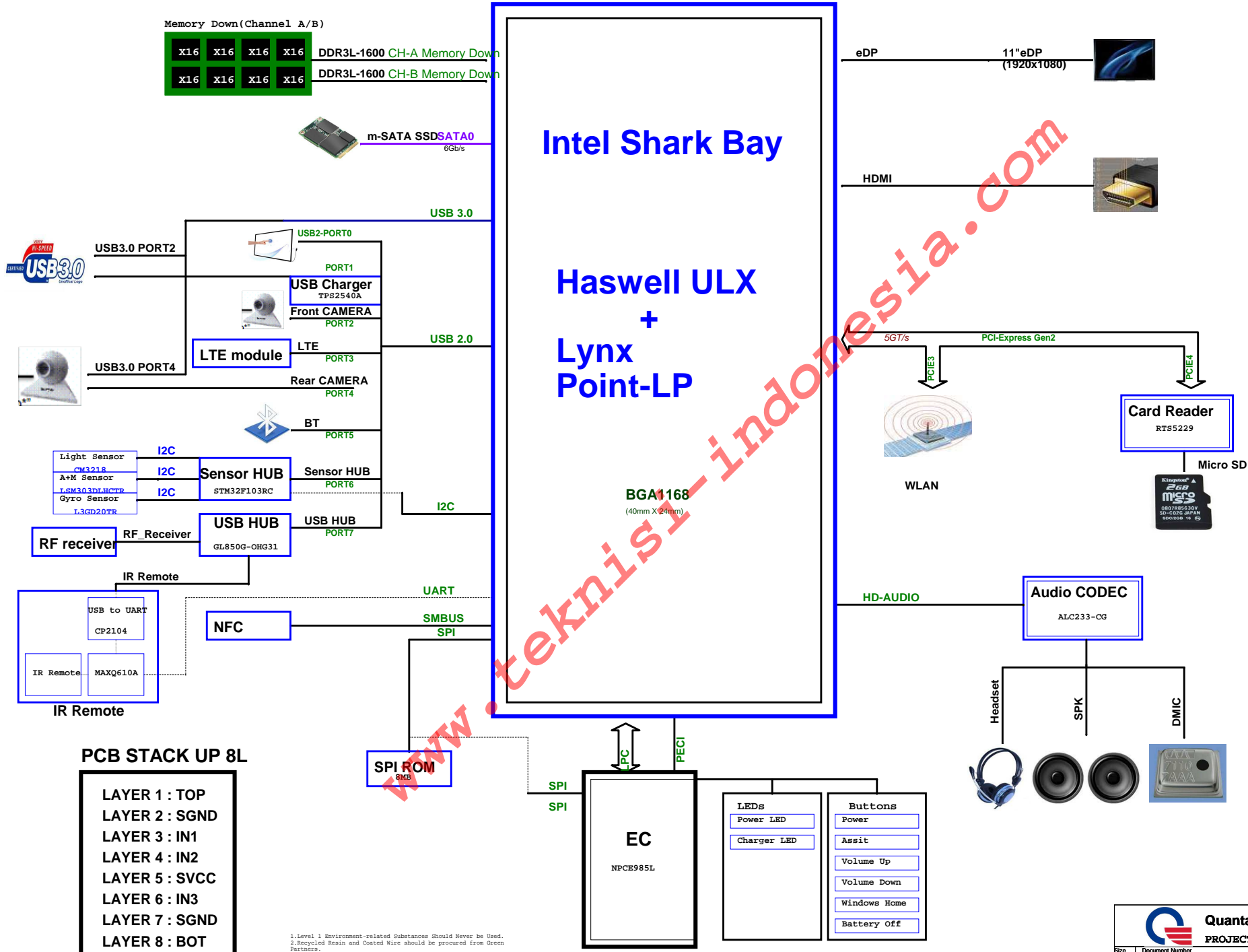


Page	Title of schematic page	Rev.	Date
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02	Block Diagram	1A	
03	Change List	1A	
04	HSW MCP(DISPLAY/eDP)	1A	
05	HSW MCP(MEMORY)	1A	
06	HSW MCP(GND/DAISY/RSVD)	1A	
07	HSW MCP(CFG)	1A	
08	HSW MCP(SIDEBAND/XDP)	1A	
09	HSW MCP(POWER)	1A	
10	HSW PCH(RTC/HDA/SATA)	1A	
11	HSW PCH(PCIE/USB)	1A	
12	HSW PCH(CLK/LPC/SPI/SMB)	1A	
13	HSW PCH(GPIO/LPIO/MISC)	1A	
14	HSW PCH (POW MANAGEMENT)	1A	
15	HSW PCH(POWER)	1A	
16	DDR3L MEMORY_x16(CH-A)	1A	
17	DDR3L MEMORY_x16(CH-B)	1A	
18	DDR3L TERMINATION	1A	
19	USB3.0	1A	
20	HDMI	1A	
21	EDP/TS	1A	
22	EC(NPCE985L)	1A	
23	mSATA (SSD)	1A	
24	WIFI/BT NGFF	1A	
25	Thermal	1A	
26	Camera	1A	
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28	Sensors Hub & Sensors	1A	
29	AUDIO(ALC233-CG)	1A	
30	Green Clork(SLG3NB3359)	1A	
31	USB2.0 Hub	1A	
32	CIR MCU(MAXQ610A-0000+)	1A	
33	USB TO UART(FT232RQ)	1A	
34	USB TO I2C(FT200XD-R)	1A	
35	Small Board	1A	
36	POWER +VCC_CORE (NCP81101)	1A	
37	POWER 3.3V/5V-NB671L/670L	1A	
38	POWER DDR3L(G5316)	1A	
39	POWER +1.05V /Thermal/+1.5V	1A	

Page	Title of schematic page	Rev.	Date
40	POWER(BAT IN / ADA IN/ UL)	1A	
41	POWER CHARGER (ISL88731C)	1A	
42	SMBUS	1A	

* : No mount

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1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

2A-1:Change value from 1K to 10K for +1.05V can't boot up.

2A-38:Remove UART interface for PCH

2A-2:Change value from 10K to 100K for +1.05V can't boot up.

2A-3:Remove TR11 for +3VPCU can't boot up.

2A-4:Remove RP15 for electrical leakage.

2A-5:Change MIC-VREFO from 30 pin to 29 pin of ALC 233.It is cover external MIC -in issue.

2A-6:Add PR37 (649K ohm) to prevent PU9 damage.

2A-7:Connecting TX signal for waking up MAX610A.

2A-8:Modifed power source to prevent TX leakage to +3V .

2A-9:Change SMI from GPIO9 to GPIO34 to meet intel's specification.

2A-10:Add 0.47uf capacitor for inrush current.(VCCDSW3_3)

2A-11:Combine rear camera board and motherboard together.

2A-12:Combine Panel and Touch Screen connectors together.

2A-13: Remove power source for HDD translate board .

2A-14: Remove +VCCIO_OUT pull high for PROCHOT.

2A-15: Prevent VCCST_PWRGD glitch during power up.

2A-16: Change clock source from crystal to clock generator

2A-17: Remove I2C interface for sensor Hub.

2A-18: Remove 0 ohm resistors for USB interface

2A-19: Change 12M from sensor hub to camera backend IC,because sensor hub doesn't prefer use clock generator.

2A-20: Add low pass filter for RF noise.

2A-21: Interchange right and left DMIC.

2A-22: For Vcore loadline fine-tune.

2A-23:For 5V_WAKE Acoustic Noise Issue.

2A-24:For KBU charger sequence issue

2A-25:For fine-tune +1.35V_SUS OCP.

2A-26:For PU9 pin11 absolute maximum ratings 6V

2A-27:For adapter OVP fine-tune.

2A-28:For +5V_WAKE and +3V_WAKE OVP fine-tune.

2A-29:Change BAT+ rating current value to 3.712A.

2A-30:Fine tune One-Shot 10ms PROCHOT# For ADP circuit.

2A-31:Because PCH_THERMTRIP# high level is only 0.7V,so we changed this circuits fto avoid H/W shutdown.

2A-32:Add connector pin for LTE voltage drop.

2A-33:Changed to 150PF for PECI error.

2A-34:Add MOSFET to prevent +3V_S5 leakage from LID# signal.

2A-35:Add WWAN PRST# Pin for BIOS detect WWAN module.

2A-36:Add capacitors for LTE RF noise.

2A-37:Add capacitors for WLAN RF noise.

1.Level 1 Environment-related Substances should never be used.
2.Reprinted Notice and Contact Wire should be prepared from Green Partners.

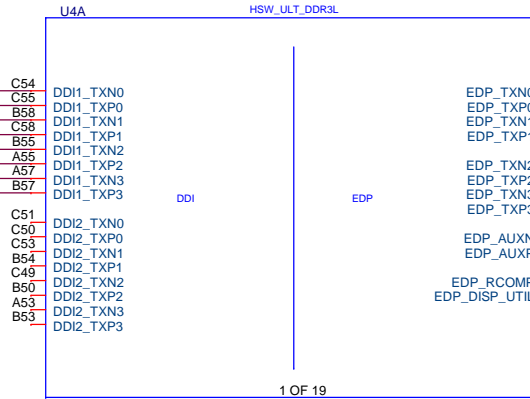
Haswell ULT (DISPLAY)

04

INT. HDMI

(20) HDMI_TXDN2
(20) HDMI_TXDP2
(20) HDMI_TXDN1
(20) HDMI_TXDP1
(20) HDMI_TXDN0
(20) HDMI_TXDP0
(20) HDMI_TXCN
(20) HDMI_TXCP

C63 1 2 0.1U/16V 4 INT_HDMI_TXN2
C64 1 2 0.1U/16V 4 INT_HDMI_TXP2
C61 1 2 0.1U/16V 4 INT_HDMI_TXN1
C62 1 2 0.1U/16V 4 INT_HDMI_TXP1
C55 1 2 0.1U/16V 4 INT_HDMI_TXN0
C57 1 2 0.1U/16V 4 INT_HDMI_TXP0
C45 1 2 0.1U/16V 4 INT_HDMI_TXCN
C49 1 2 0.1U/16V 4 INT_HDMI_TXCP



EDP_TXN0 (21)
EDP_TXP0 (21)
EDP_TXN1 (21)
EDP_TXP1 (21)

EDP_TXN2
EDP_TXP2
EDP_TXN3
EDP_TXP3

EDP_AUXN (21)
EDP_AUXP (21)

EDP_COMP
DP_UTIL
R206 *0.4 EDP_BLPWM
R207 *0.4 NC

EDP_COMP MUST PU VCCIOA_OUT

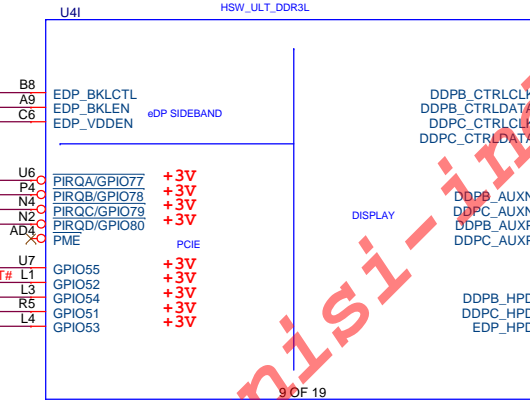
R218 24.9/F 4

+VCCIOA_OUT

(21) EDP_BLPWM
(22) EDP_BLEN
(21) EDP_VDDEN

(13) MPCIE_RST_N
(13) PCH_GPIO78
(13) PCH_GPIO79
(13) PCH_GPIO80

(13) TOUCHPAD_INTR#
(13) TOUCH_PANEL_RST#
(13) PCH_GPIO54
(13) PCH_GPIO53



HDMI_SCL (20)
HDMI_SDA (20)

DDPB_AUXN
DDPB_AUXP
DDPC_AUXN
DDPC_AUXP

HDMI_HPD_Q (20)
EDP_HPD (21)

R210 100K_4

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

DDR3L Single /Dual Channel Strap

	High	Low
DRAM_CH_SEL	Single	Dual

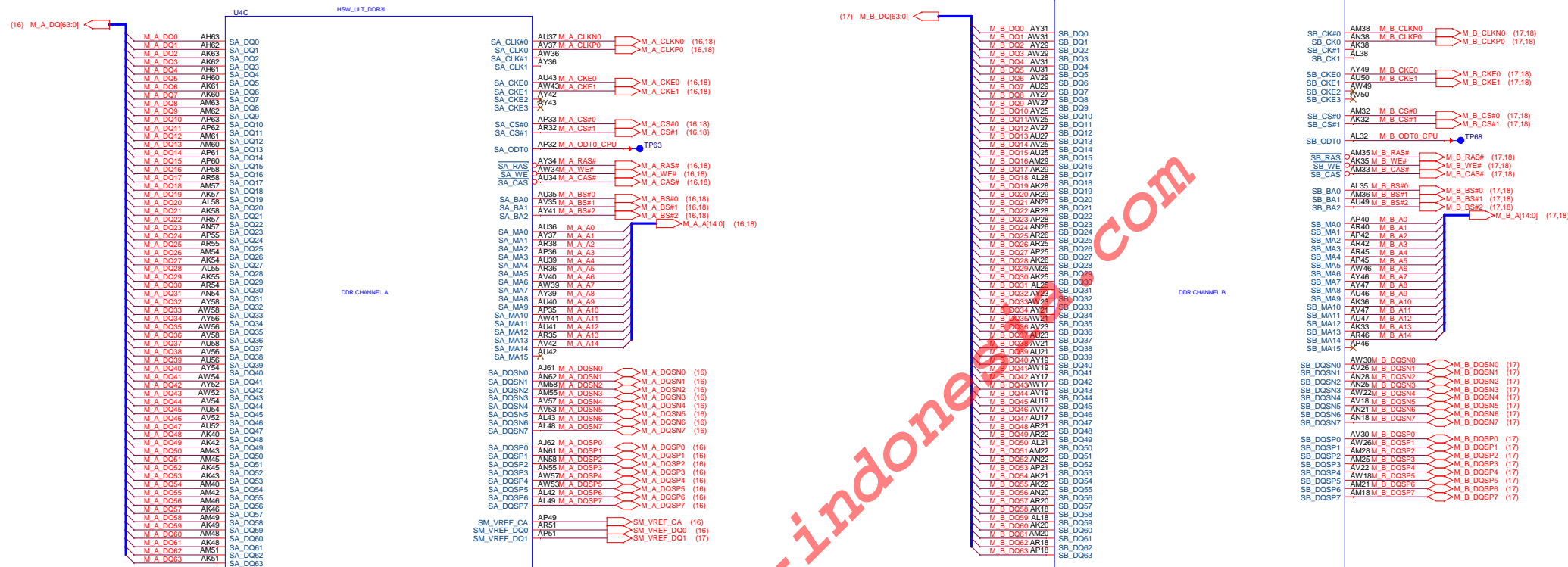


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Haswell ULT (DDR3L)



1. Level 1 Environment-related Substances should Never be Used.
2. Recycled Resin and Coated Wire should be procured from Green Suppliers.



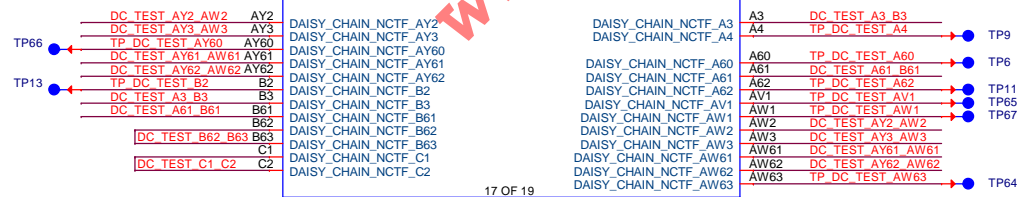
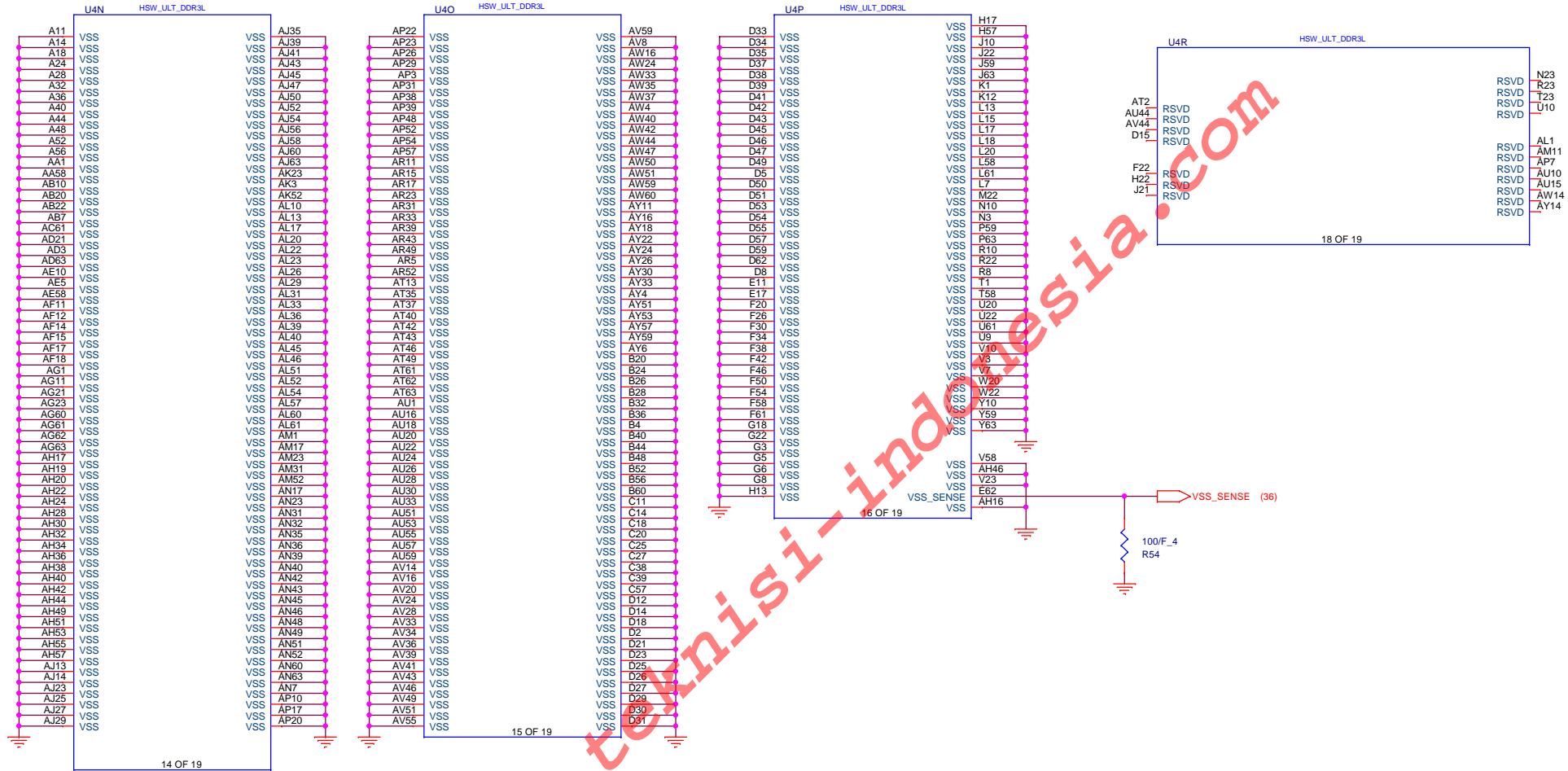
Quanta Computer Inc.

PROJECT : KR1

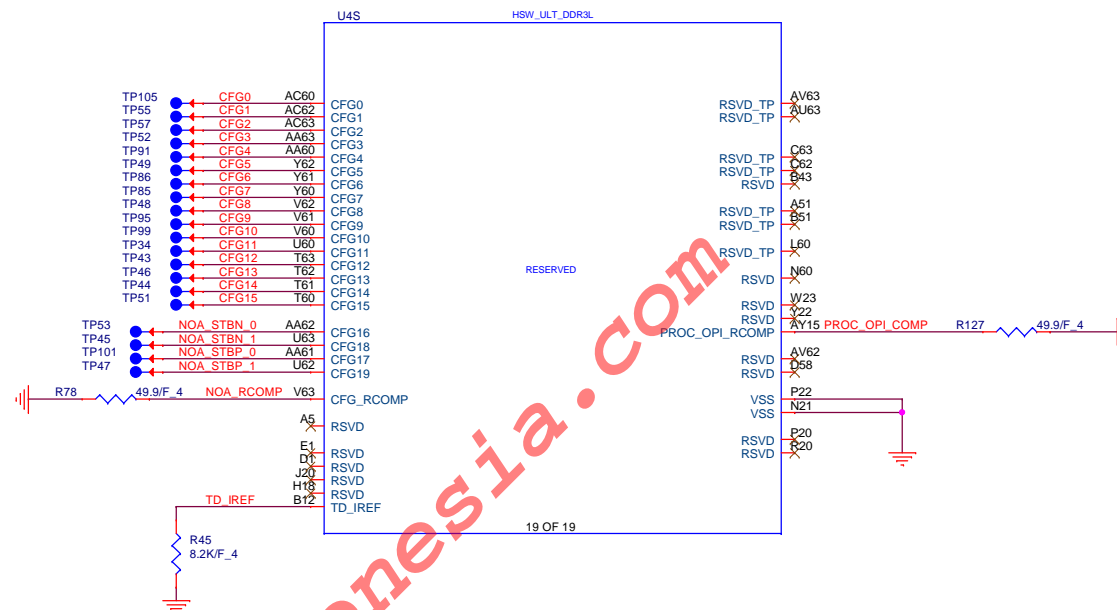
Size Document Number Rev 1A
HWS MCP(Memory)
Date: Monday, May 13, 2013 Sheet 5 of 44

Haswell ULT (GND)

06



1.Level 1 Environment-related Substances should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.



Processor Strapping

	1	0	
CFG0 EAR-STALL/NOT STALL RESET SEQUENCE AFTER PCU PLL IS LOCKED	(DEFAULT) NORMAL OPERATION; NO STALL	STALL	CFG0 R232 *1K 4
CFG1 PCH/ PCH LESS MODE SELECTION	(DEFAULT) NORMAL OPERATION	PCH-LESS MODE	CFG1 R90 *1K 4
CFG3 PHYSICAL_DEBUG_ENABLED (DFX PRIVACY)	DISABLED	ENABLED SET DFX ENABLED BIT IN DEBUG INTERFACE MSR	CFG3 R86 *1K 4
CFG4 DISPLAY PORT PRESENCE STRAP	DISABLED NO PHYSICAL DISPLAY PORT ATTACHED TO EMBEDDED DISPLAY PORT	ENABLED AN EXTERNAL DISPLAY PORT DEVICE IS CONNECTED TO THE EMBEDDED DISPLAY PORT	CFG4 R230 *1K 4
CFG 8 ALLOW THE USE OF NOA ON LOCKED UNITS	DISABLED(DEFAULT); IN THIS CASE, NOA WILL BE DISABLED IN LOCKED UNITS AND ENABLED IN UN-LOCKED UNITS	ENABLED; NOA WILL BE AVAILABLE REGARDLESS OF THE LOCKING OF THE UNIT	CFG8 R83 *1K 4
CFG9 NO SVID PROTOCOL CAPABLE VR CONNECTED	VRS SUPPORTING SVID PROTOCOL ARE PRESENT	NO VR SUPPORTING SVID IS PRESENT. THE CHIP WILL NOT GENERATE (OR RESPOND TO) SVID ACTIVITY	CFG9 R225 *1K 4
CFG10 SAFE MODE BOOT	POWER FEATURES ACTIVATED DURING RESET	POWER FEATURES (ESPECIALLY CLOCK GATINE ARE NOT ACTIVATED	CFG10 R227 *1K 4

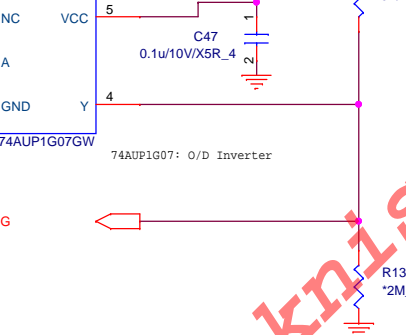
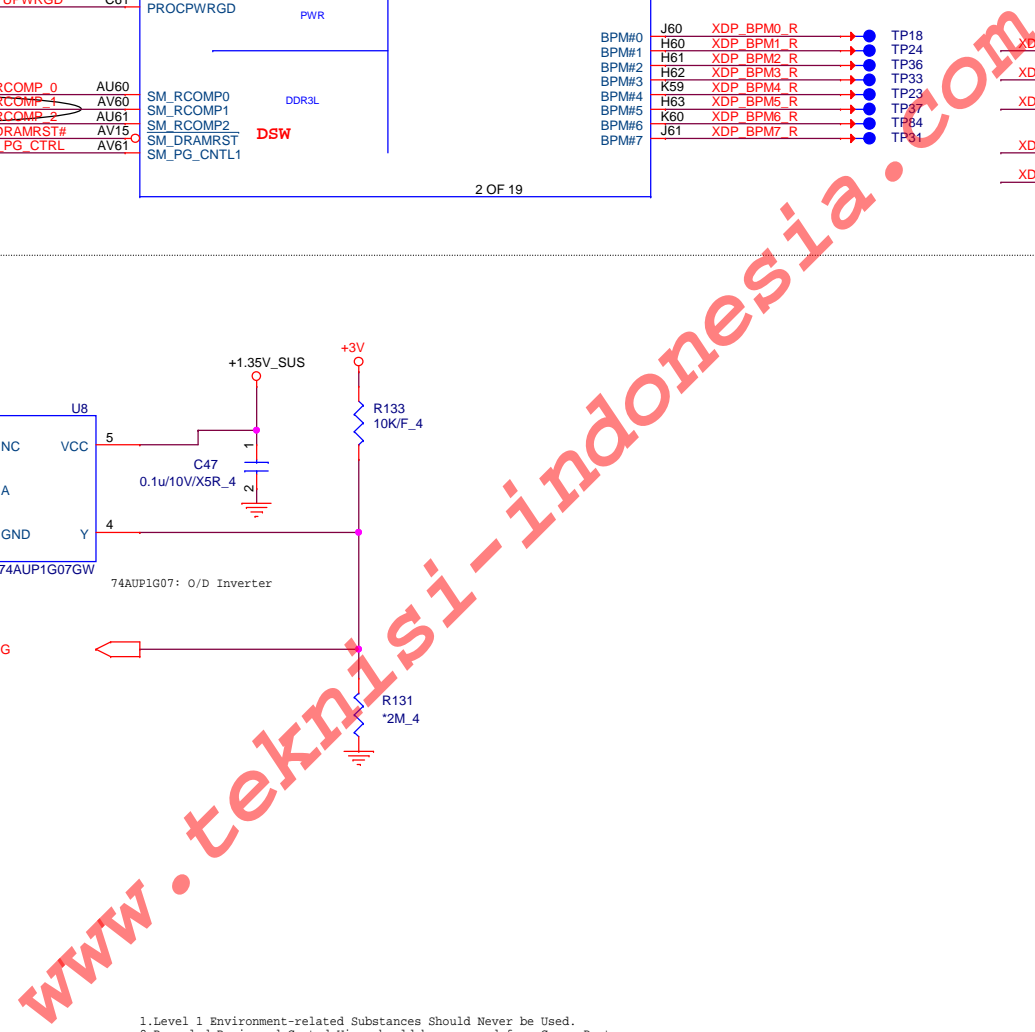
1. Level 1 Environment-related Substances Should Never be Used.
2. Recycled Resin and Coated Wire should be procured from Green Partners.



Quanta Computer Inc.

PROJECT : KR1

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	HSW MCP(CFG)	1A
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74AUP1G07: O/D Inverter

C47
0.1u/10V/X5R_4

R131
*2M_4

VCC

GND

Y

4

5

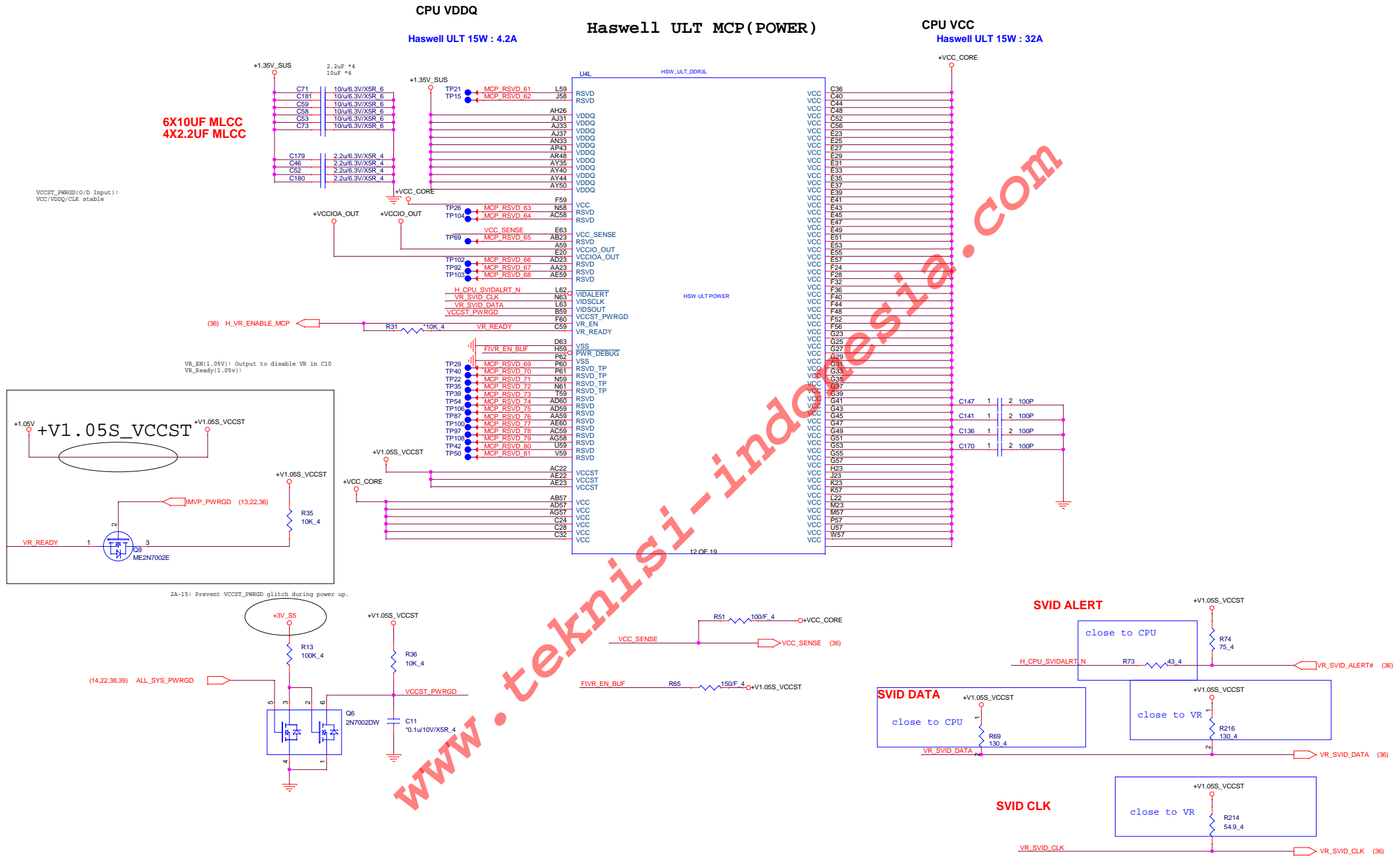
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2

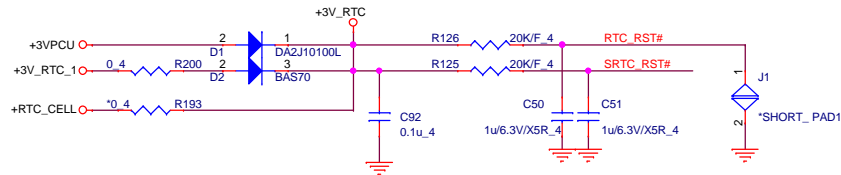
3

G

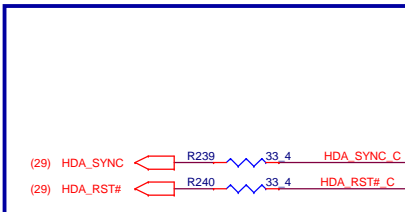
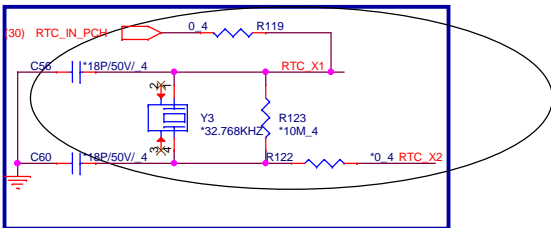

```
Haswell ULT MCP(Power)
```



RTC Power trace width 20mils.

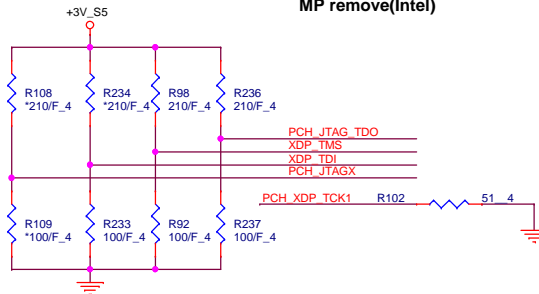


2A-16: Change clock source from crystal to clock generator



PCH JTAG Debug (CLG)

MP remove(Intel)



PCH Strap Table

Pin Name	Strap description	Sampled	Configuration	note
SPKR	No reboot mode setting	PWROK	0 = Default (weak pull-down 20K) 1 = Setting to No-Reboot mode	+3V R79 *1K 4 HDA_SPKR (13,29)
HDA_SDO	Flash Descriptor Security Override / Intel ME Debug Mode	PWROK	0 = Security Effect (Int PD) 1 = Can be Override	+3V_S5 R120 *1K 4 HDA_SDOIN_C
INTVRMEN	Integrated 1.05V VRM enable	ALWAYS	Should be always pull-up	+3V_RTC R128 330K 4 PCH_INTVRMEN R116 *330K 4

Haswell ULT (RTC, HDA, JTAG, SATA)

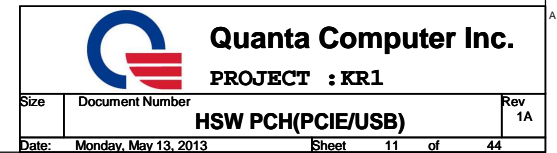


SSD

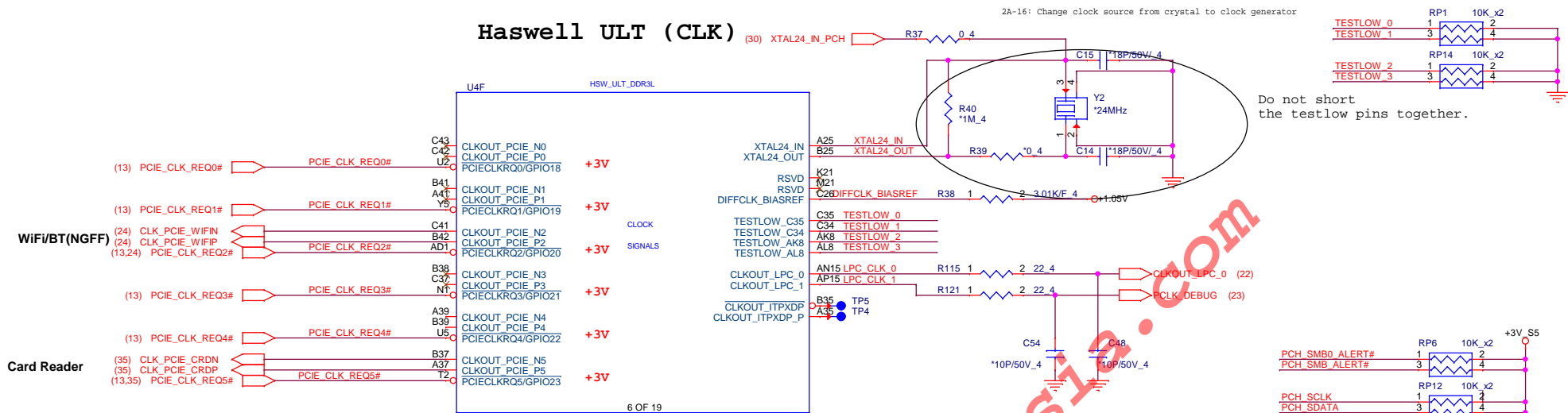
Card Reader

1. Level 1 Environment-related Substances Should Never be Used.
2. Recycled Resin and Coated Wire should be procured from Green Partners.

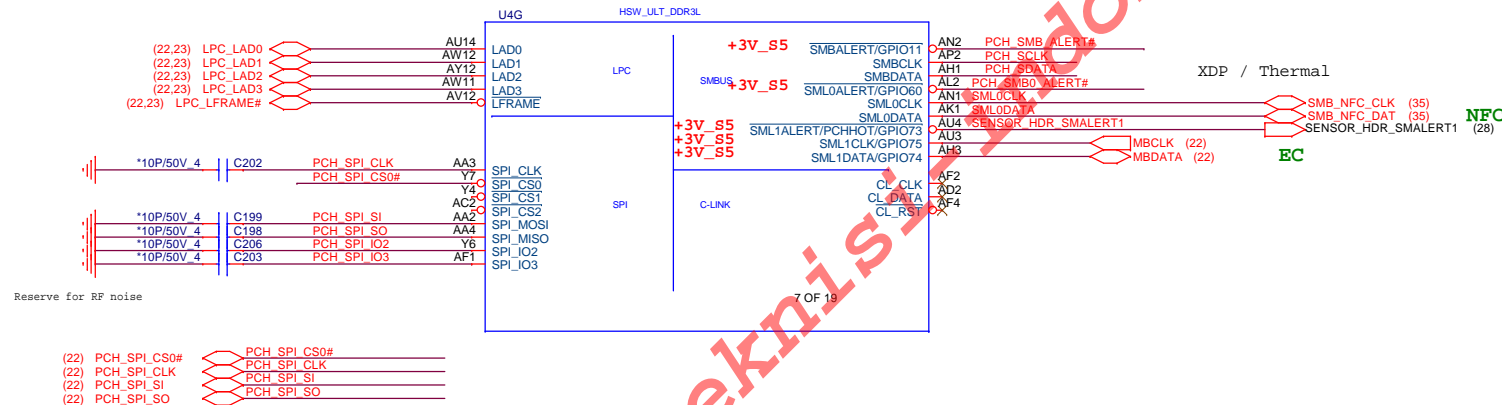
		Quanta Computer Inc. PROJECT : KR1	
		HSW PCH(RTC/HDA/SATA)	
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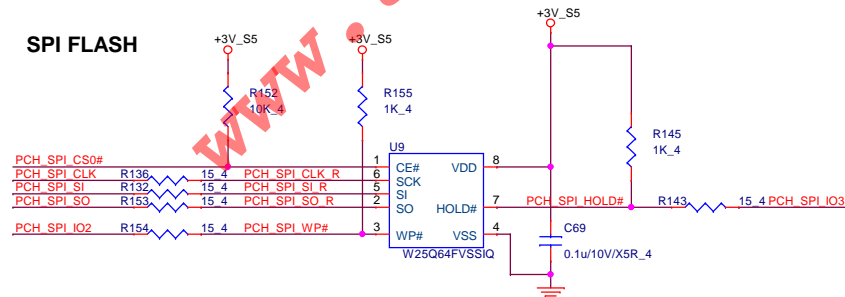
Haswell ULT (CLK)



Haswell ULT (LPC/SPI/SMB/CLINK)



For EC load code from BIOS flash ROM



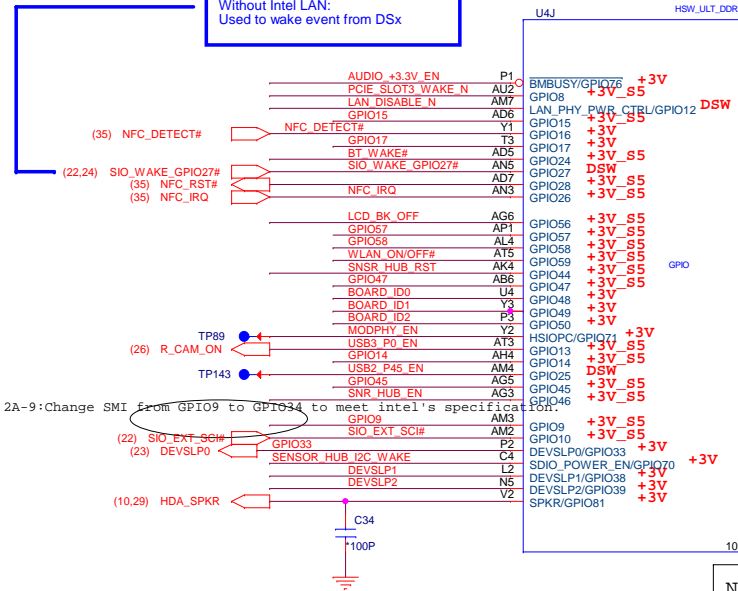
- 1.Level 1 Environment-related Substances Should Never be Used.
- 2.Recycled Resin and Coated Wire should be procured from Green Partners

TLS CONFIDENTIALITY STRAP(GPIO15)		
NC	Default	
PU	EN	

Hasswell ULT(GPIO,LPIO,MISC)

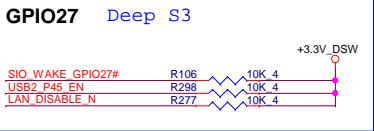
GPIO27

With Intel LAN:
Connect to LANWAKE# pin on the LAN
Without Intel LAN:
Used to wake event from DSx

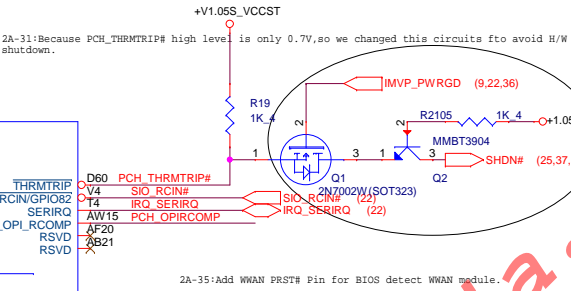


No Reboot Strap(GPIO81)		
NC	Default	
PU	EN	

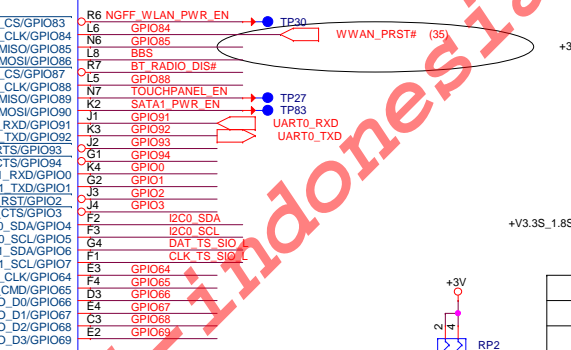
Vendor	Vendor Part Number	BOARD_ID0	BOARD_ID1	BOARD_ID2
Samsung (4G)	K4B4G1646B-HYK0	0	0	0
Hynix (4G)	H5TC4G63AFR-PBA	0	0	1
Elpida (4G)	EDJ4216EFBG-GN-F	0	1	0
Samsung (8G)		0	1	1
Hynix (8G)		1	0	0
Elpida (8G)		1	0	1
		1	1	0
		1	1	1



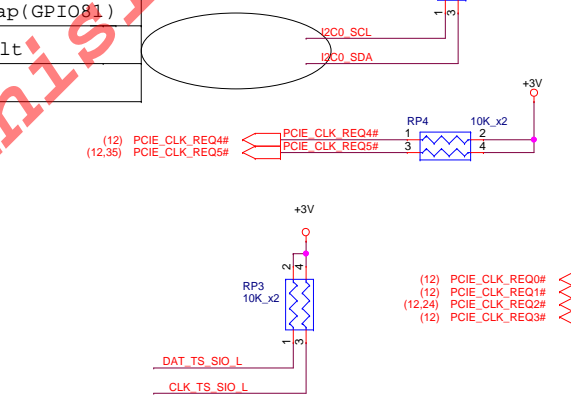
2A-31:Because PCH_THRMTRIP# high level is only 0.7V,so we changed this circuits fto avoid H/W shutdown.



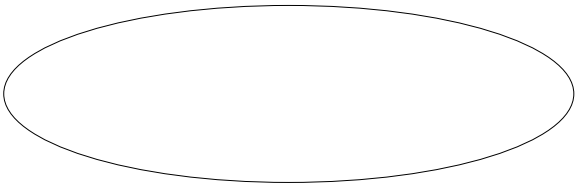
2A-35:Add WWAN PRST# Pin for BIOS detect WWAN module.



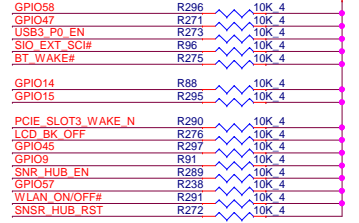
2A-17: Remove I2C interface for sensor Hub.



2A-31:Because PCH_THRMTRIP# high level is only 0.7V,so we changed this circuits fto avoid H/W shutdown.

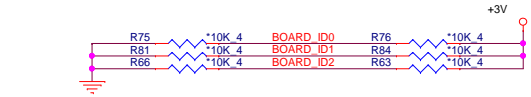
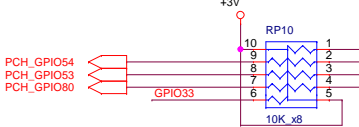
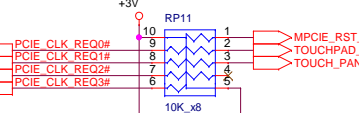
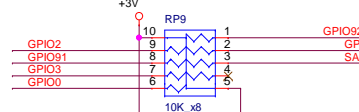
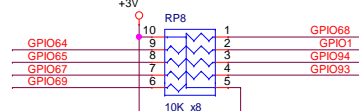


GPIO Pull-up/Pull-down(CLG)



GPIO86	
PU	LPC
PD	SPI (Default IPD)

GPIO66	
R1547	ENABLE
R1547_NC	DISABLE(Default)

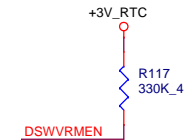


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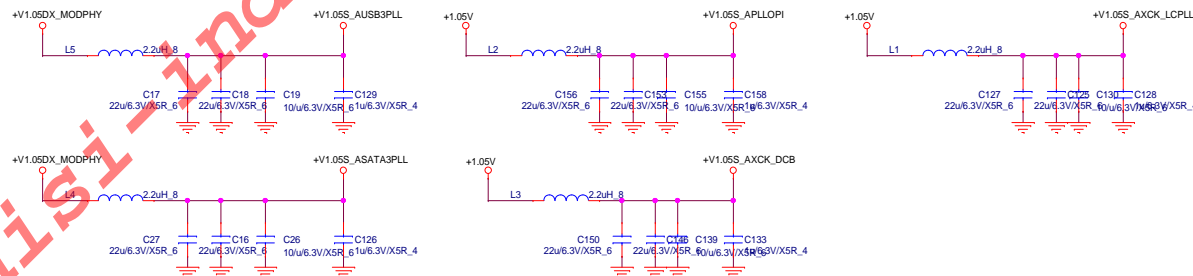
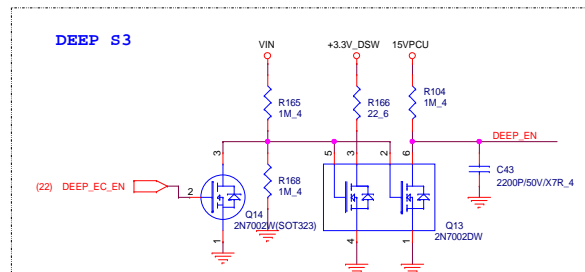
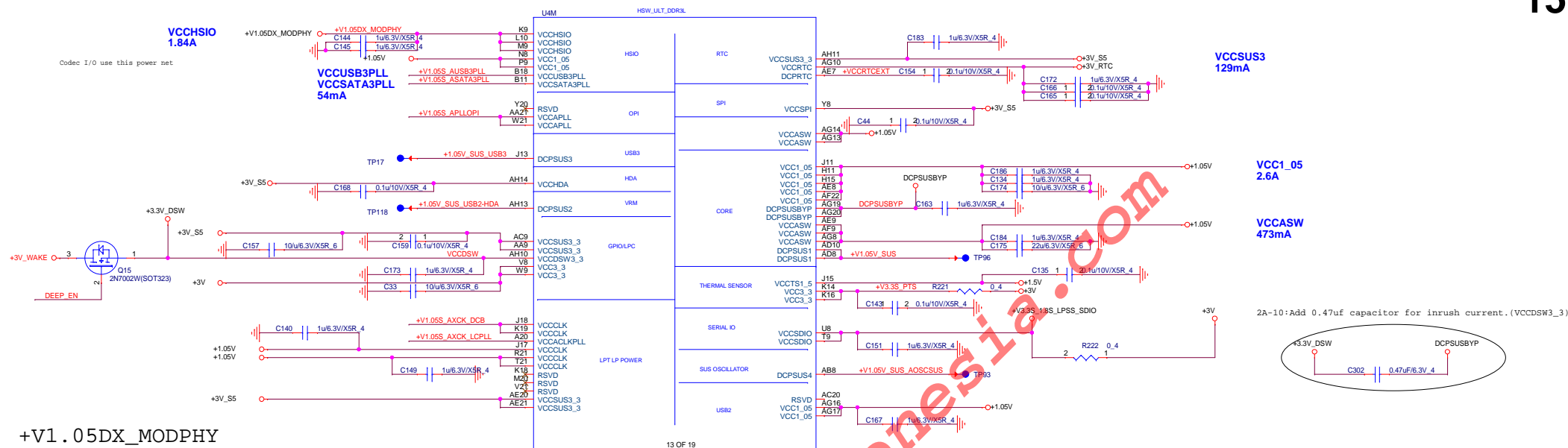
PROJECT : KR1

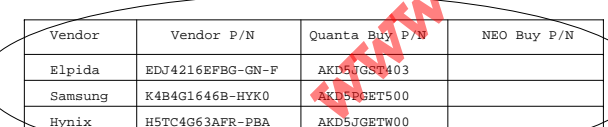
Size	Document Number	Rev 1A
HSW PCH(GPIO/MISC)		
Date:	Monday, May 13, 2013	Sheet 13 of 44

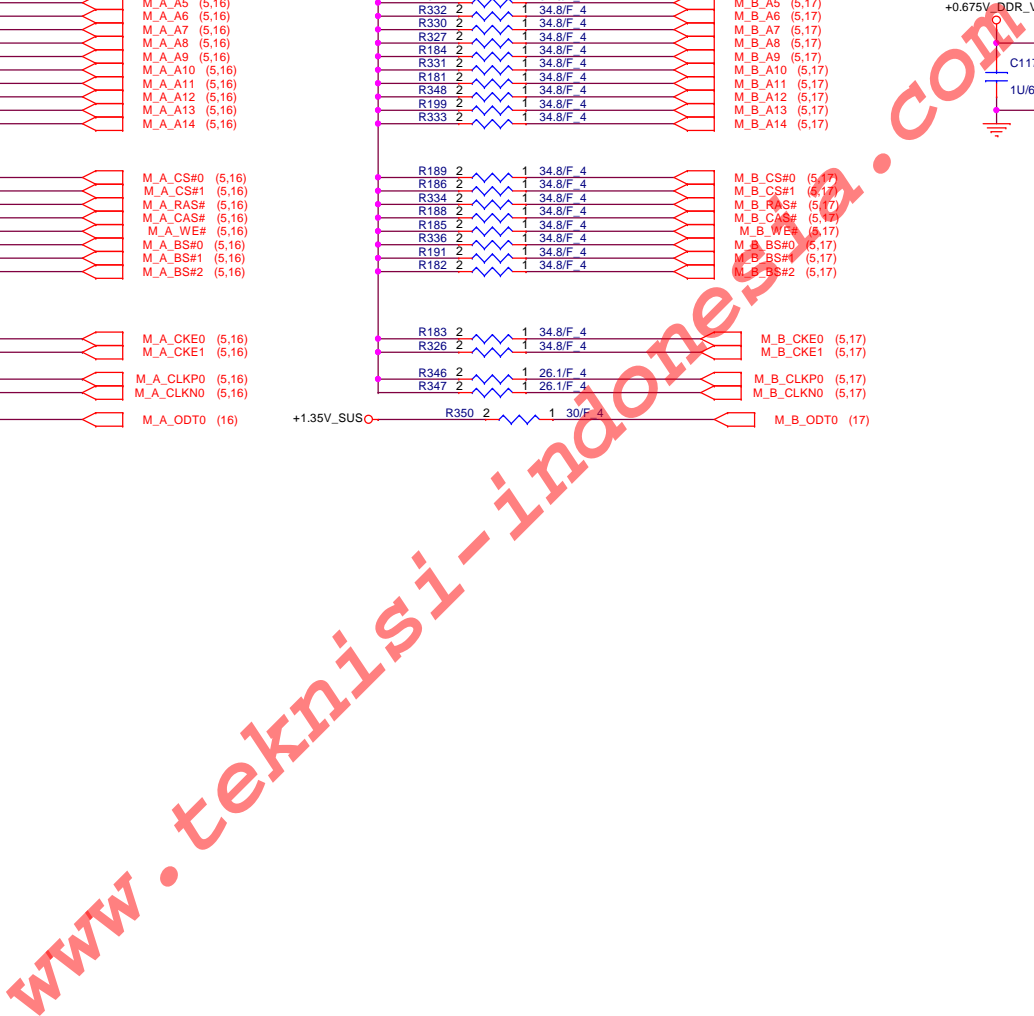
1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.



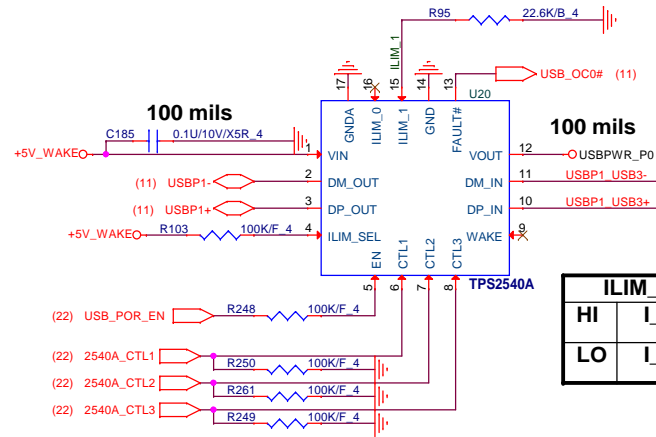
On Die DSW VR Enable
High = Enable (Default)
Low = Disable





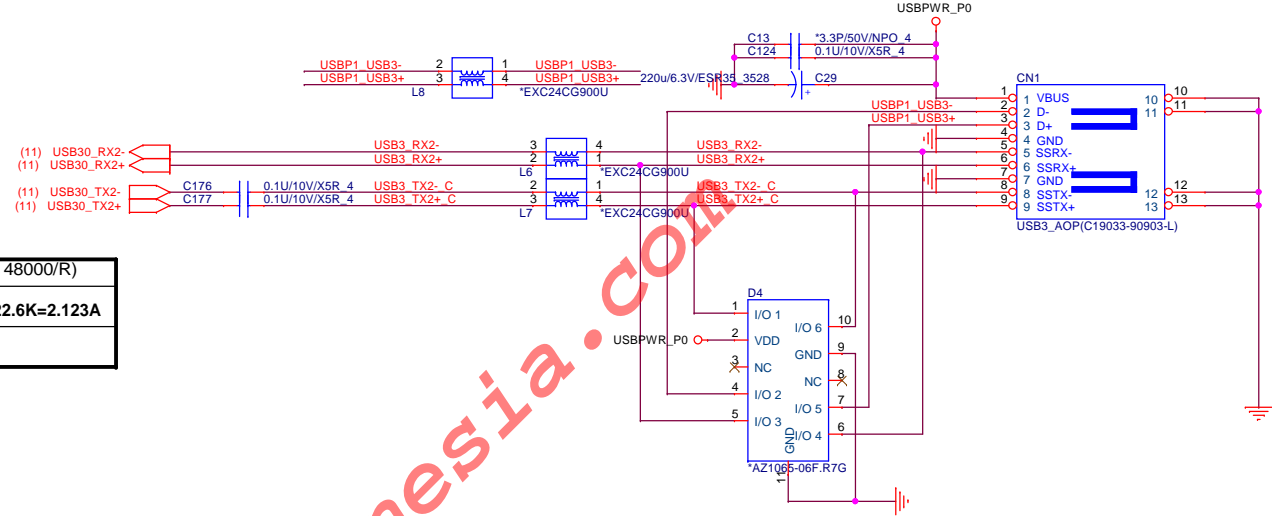


USB Charger



ILIM_SEL (I LIMIT(A)= 48000/R)		
HI	I_LIM_1	48000/22.6K=2.123A
LO	I_LIM_0	

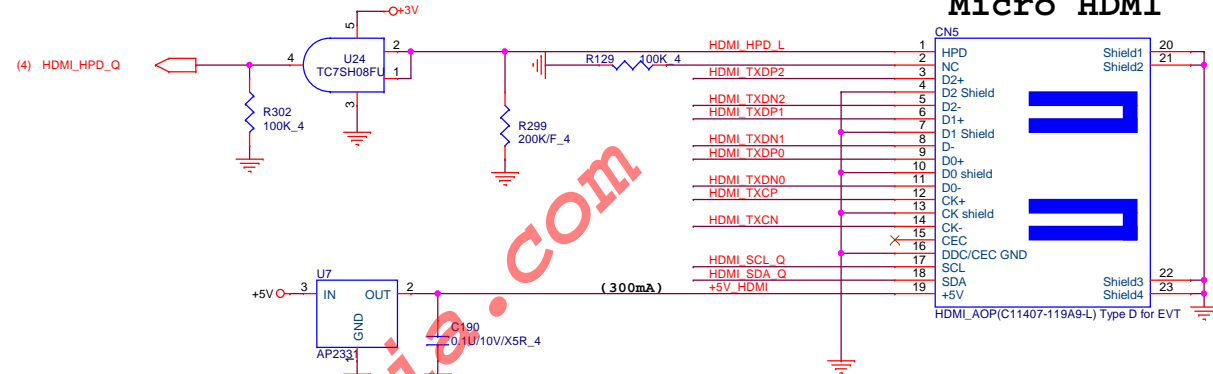
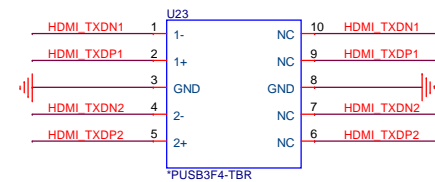
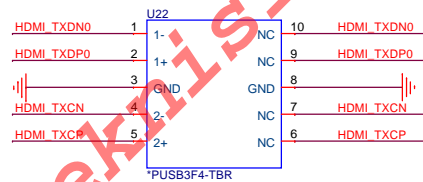
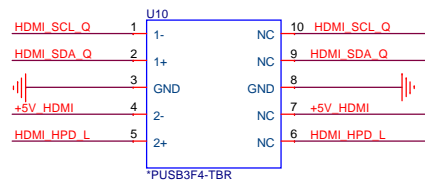
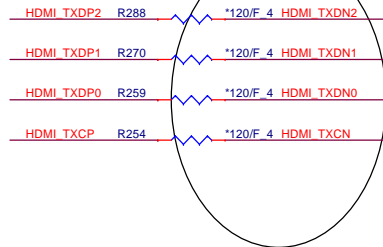
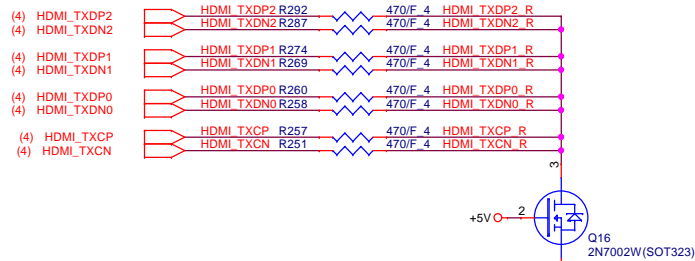
USB 3.0 PORT0



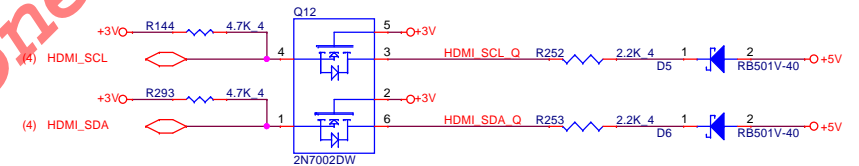
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For HDMI Dongle



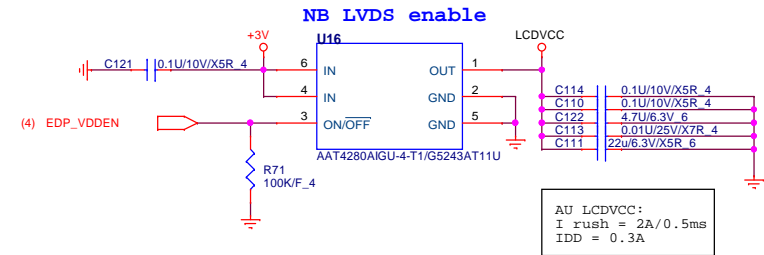
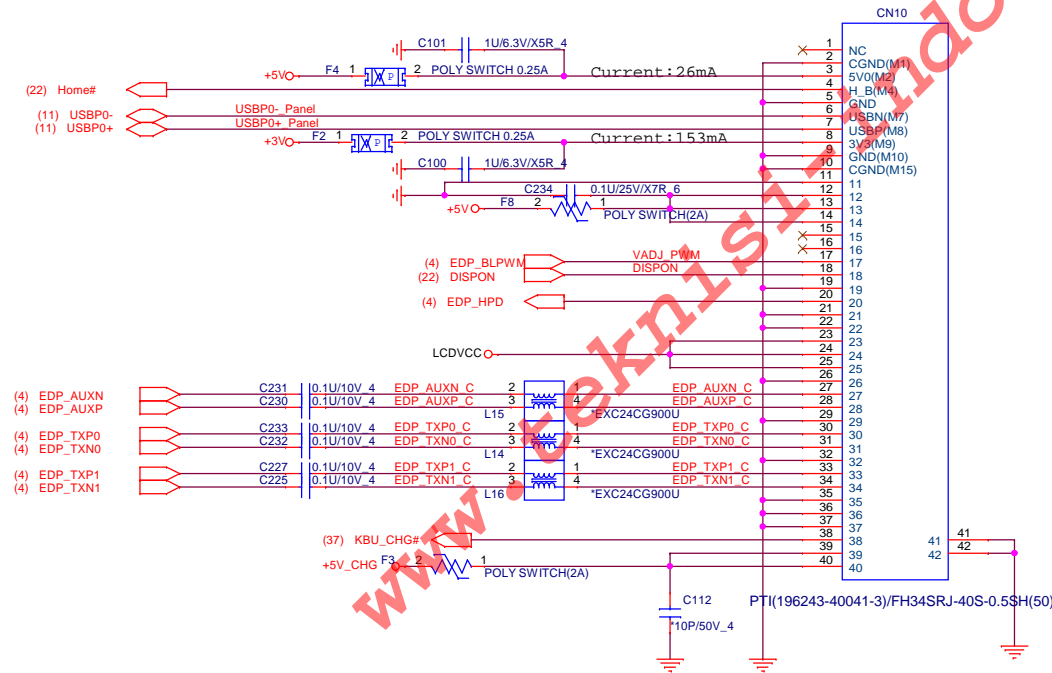
1.Level 1 Environment-related Substances Should Never be Used.
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2A-12:Combine Panel and Touch Screen connectors together.

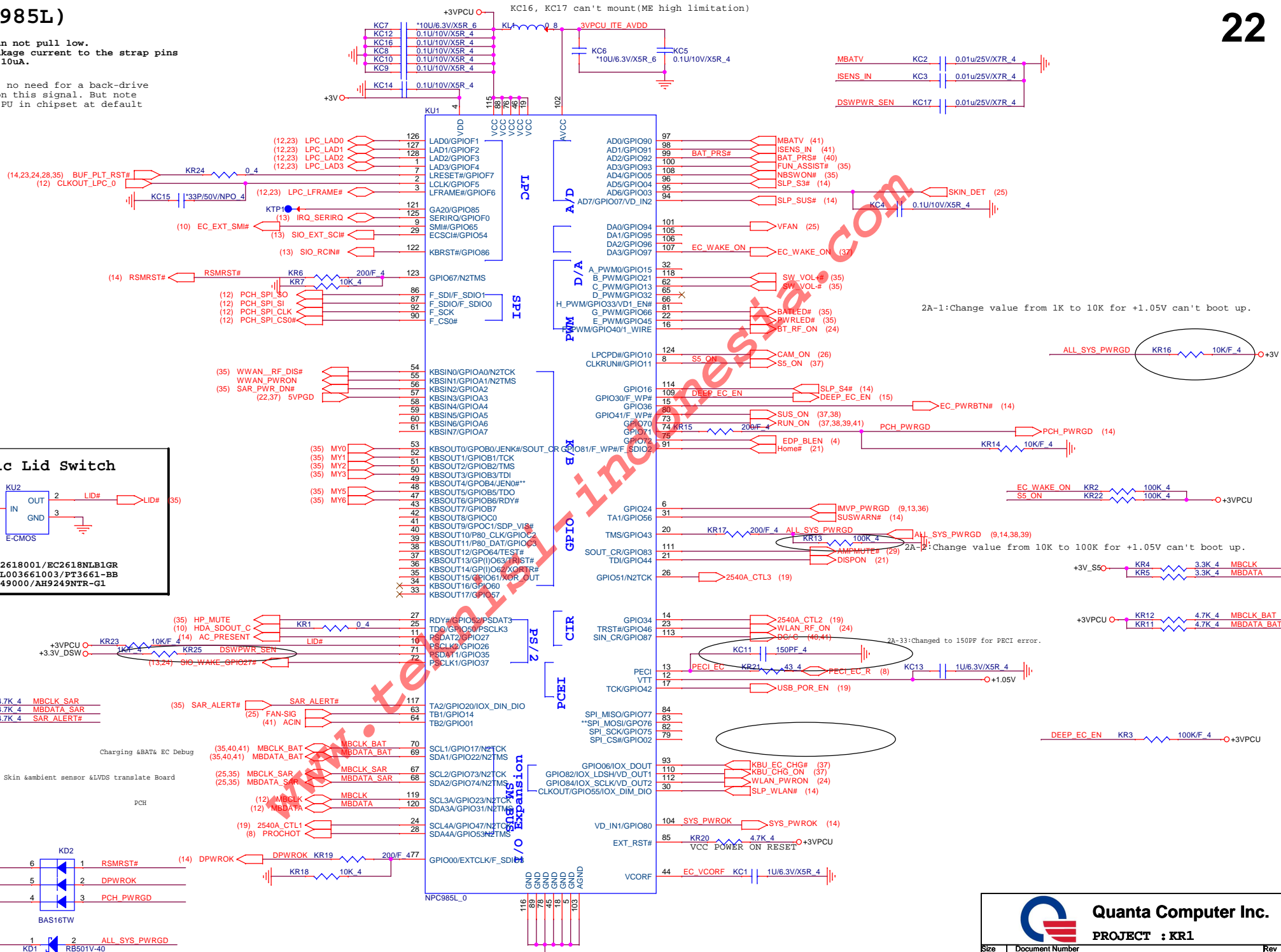
Panel & Touch Screen



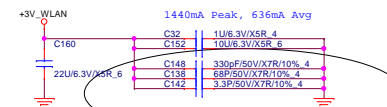
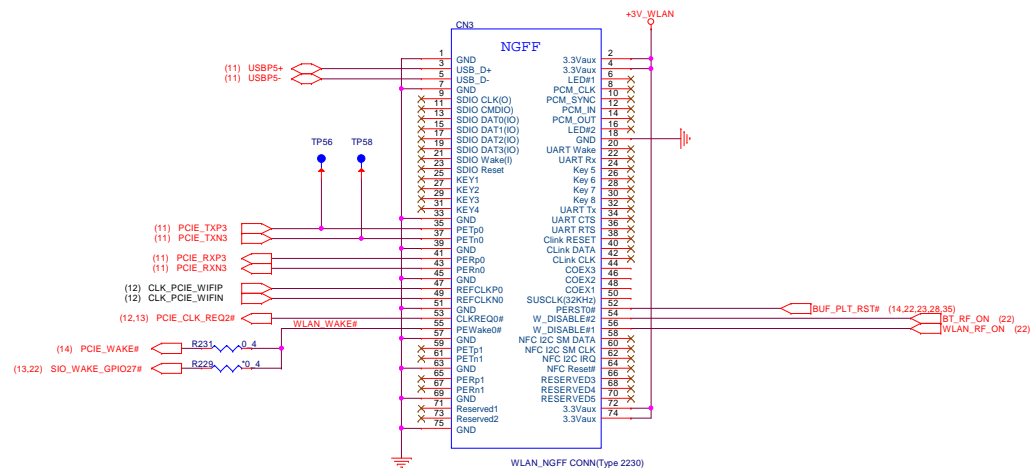
EC (NPCE985L)

**** Strapping Pin, Can not pull low.**
Note the input leakage current to the strap pins must be less than 10uA.

Since ECSCI is OD, no need for a back-drive protection diode on this signal. But note there is internal PU in chipset at default

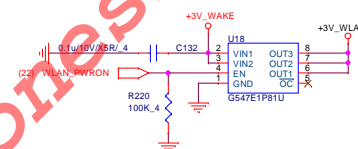


NGFF Wifi/BT connector



2A-37: Add capacitors for WLAN RF noise.

add



AC Mode : Support Wake on WLAN
DC Mode : Don't support wake on WLAN

Level 1 Environment-related Substances Should Never be Used.
Recycled Resin and Coated Wire should be procured from Green Partners.



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PROJECT : KR1

Size Document Number

WIFI/BT NGFF

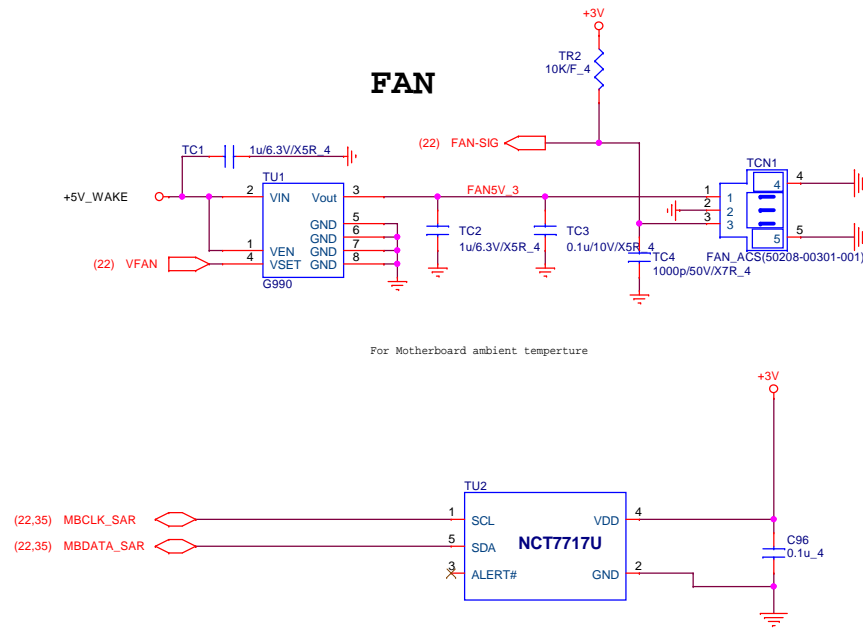
Date: Monday, May 13, 2013

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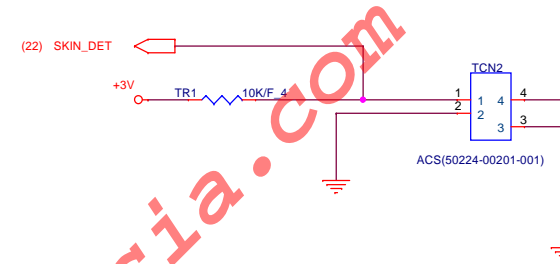
Rev

1A

FAN

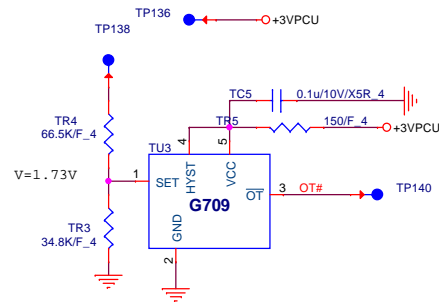


Add Thermal sensor for Skin tempertuature



H/W Thermal Protect

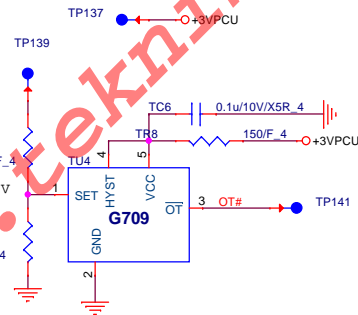
Ambient Sensor



$$RSET(k\Omega) = 0.0012T2 - 0.9308T + 96.147$$

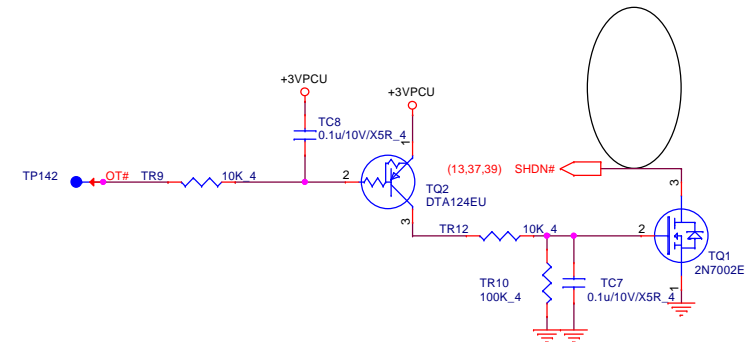
75	33.0K
95	18.5K
100	15K
107	10.3K
110	8.2K

CPU Thermal Sensor

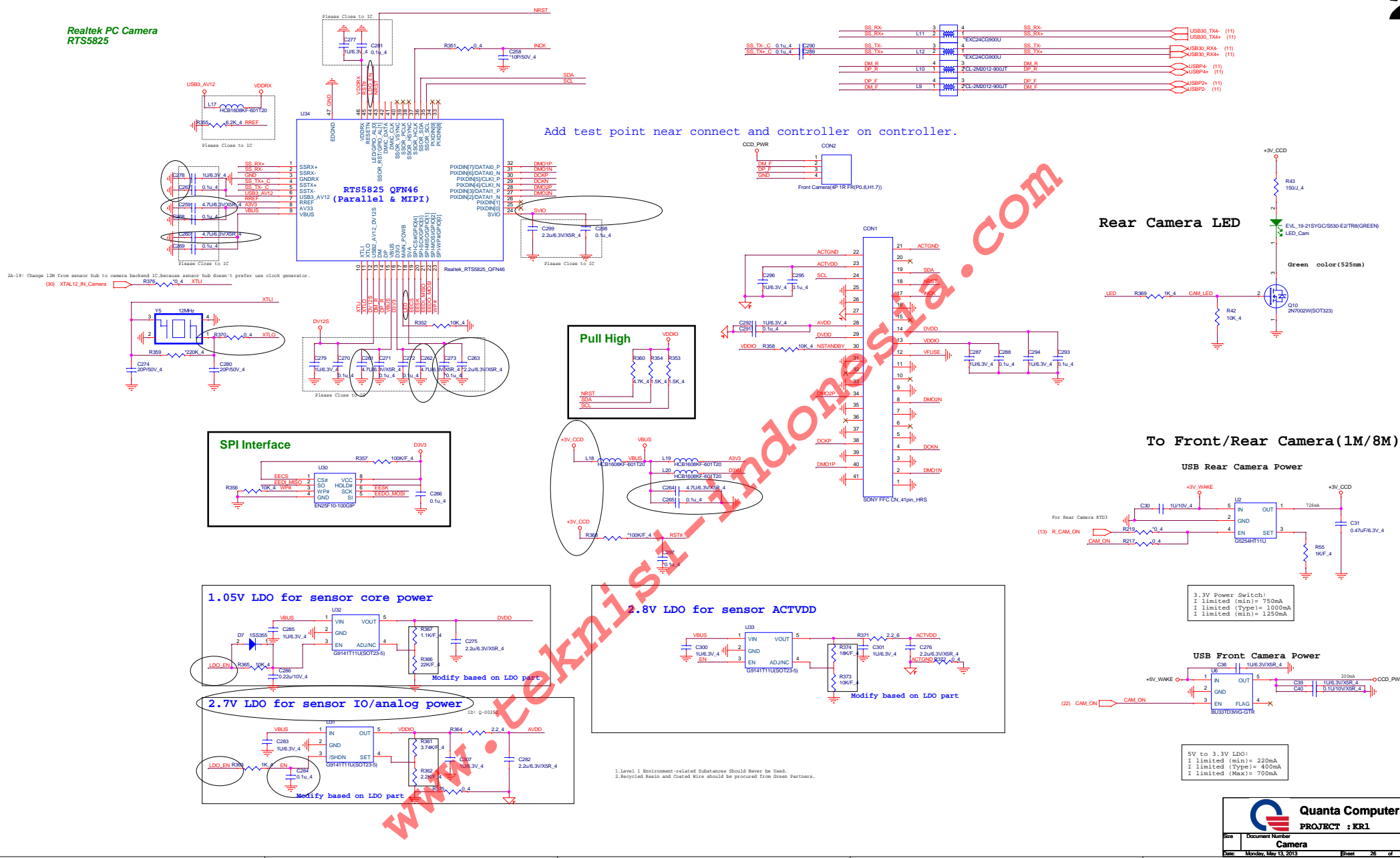


TP Szie: TP3075(Request from Production Line)

2A-3:Remove TR11 for +3VPCU can't boot up.

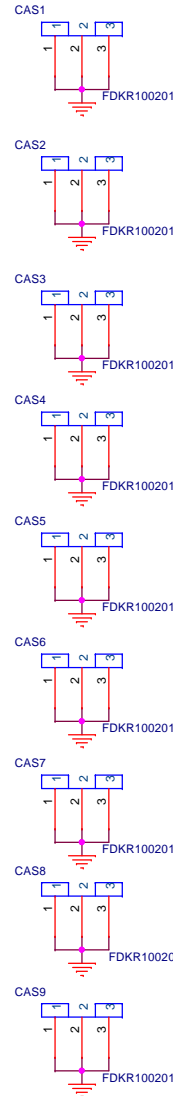


Realtek PC Camera RTS5625

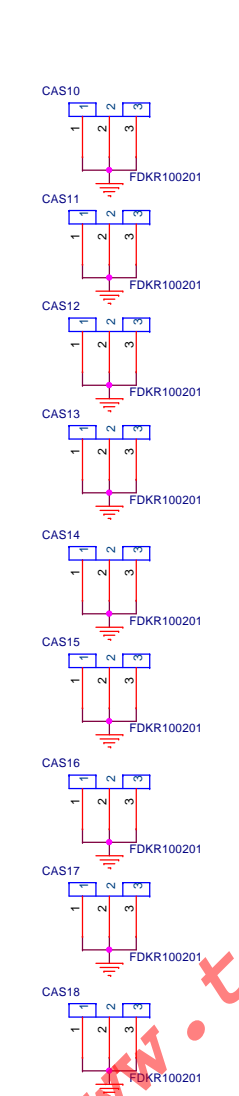


Shielding Case

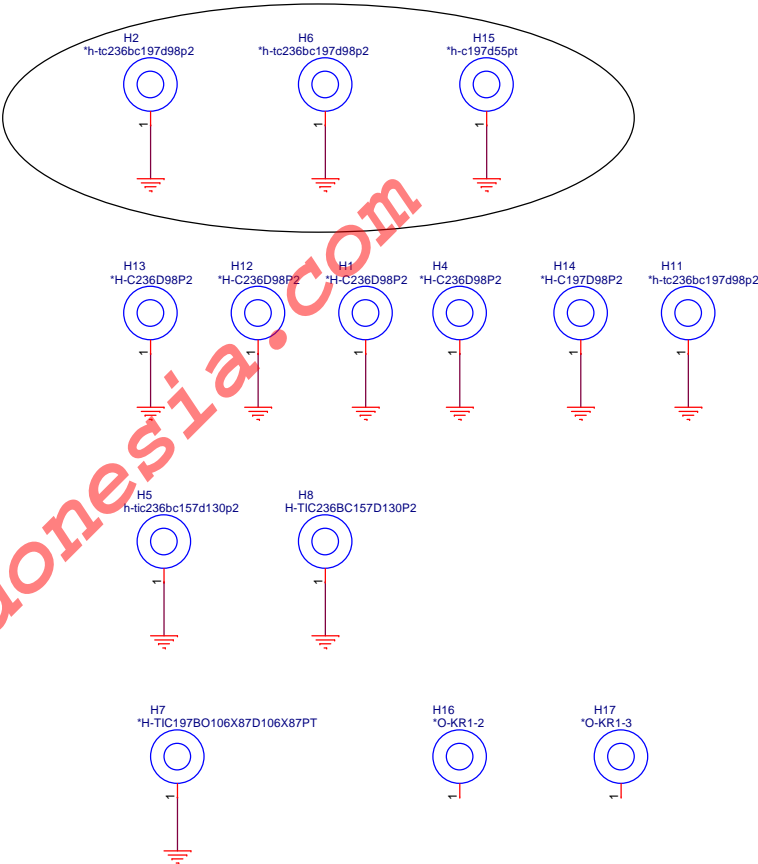
TOP Side



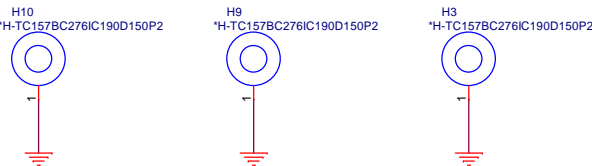
Bottom Side



Screw Hole



CPU Breaket Screw Hole

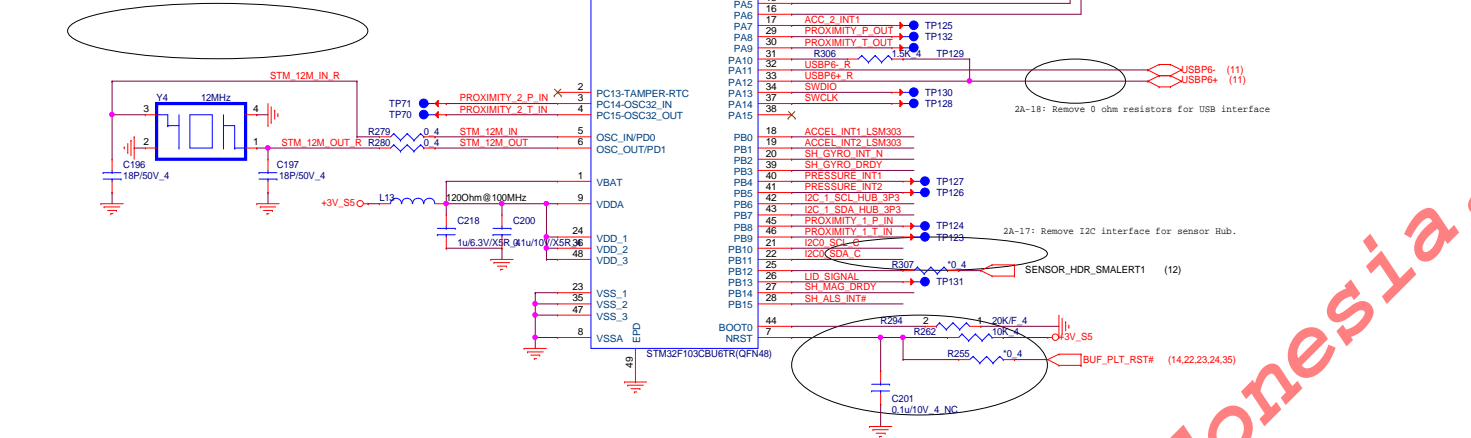


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1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Devices	LSM303DLHC			L3GD20TR		
Strap Pins	PA1	PA2	PA3	PA4	PA5	PA6
	1	0	1	0	1	1

2A-19: Change 12M from sensor hub to camera backend IC, because sensor hub doesn't prefer use clock generator.



2A-18: Remove 0 ohm resistors for USB interface

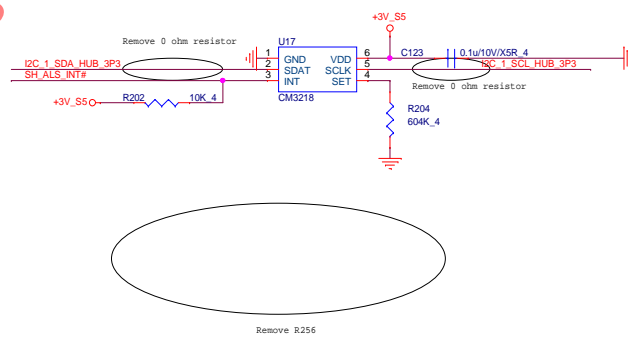
2A-17: Remove I2C interface for sensor Hub.

SENSOR_HDR_SMALET1 (12)

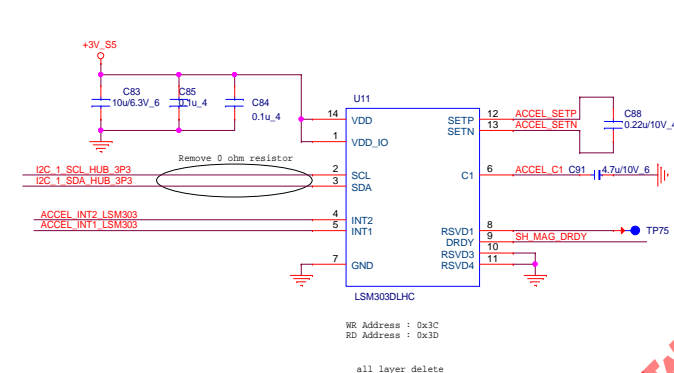
BUF_PLT_RST# (14,22,23,24,35)

2A-4: Remove RP15 for electrical leakage.

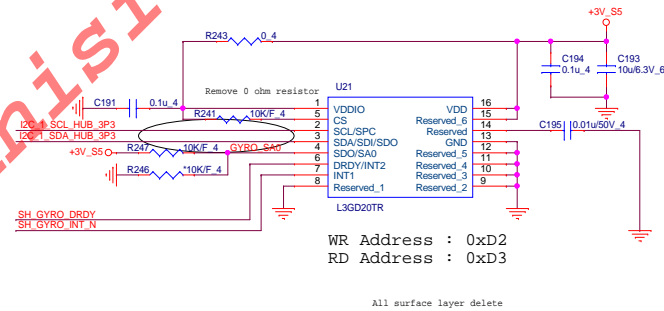
Ambient Light Sensor



G-sensor/E-compass/Magnetometer



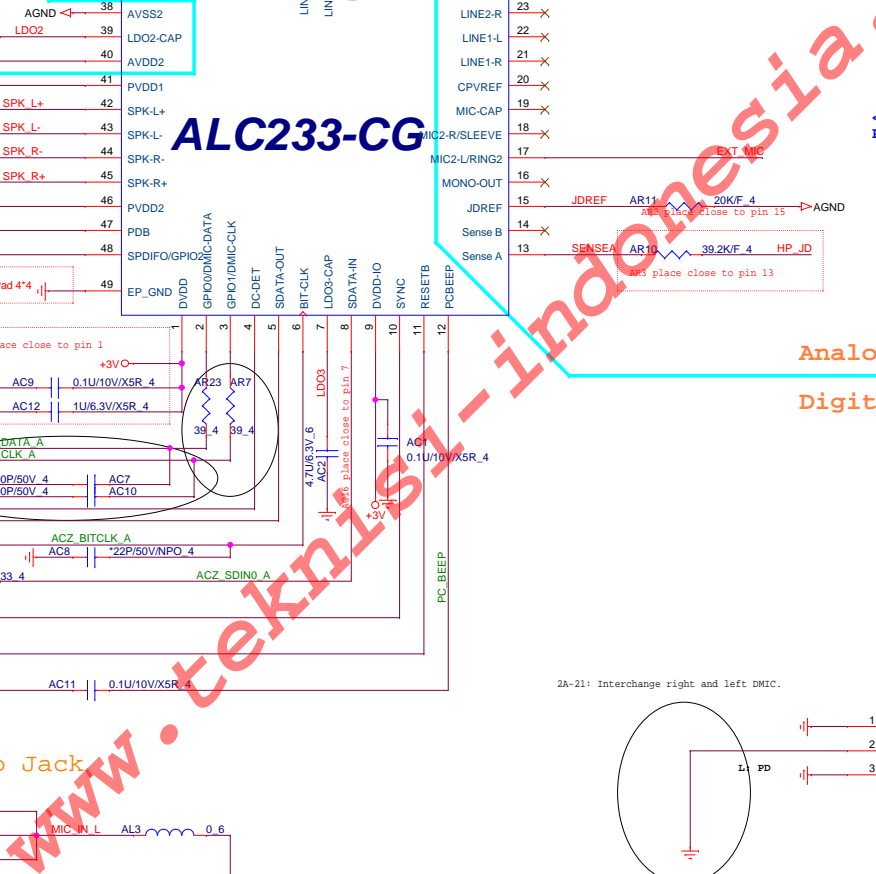
Gyroscope




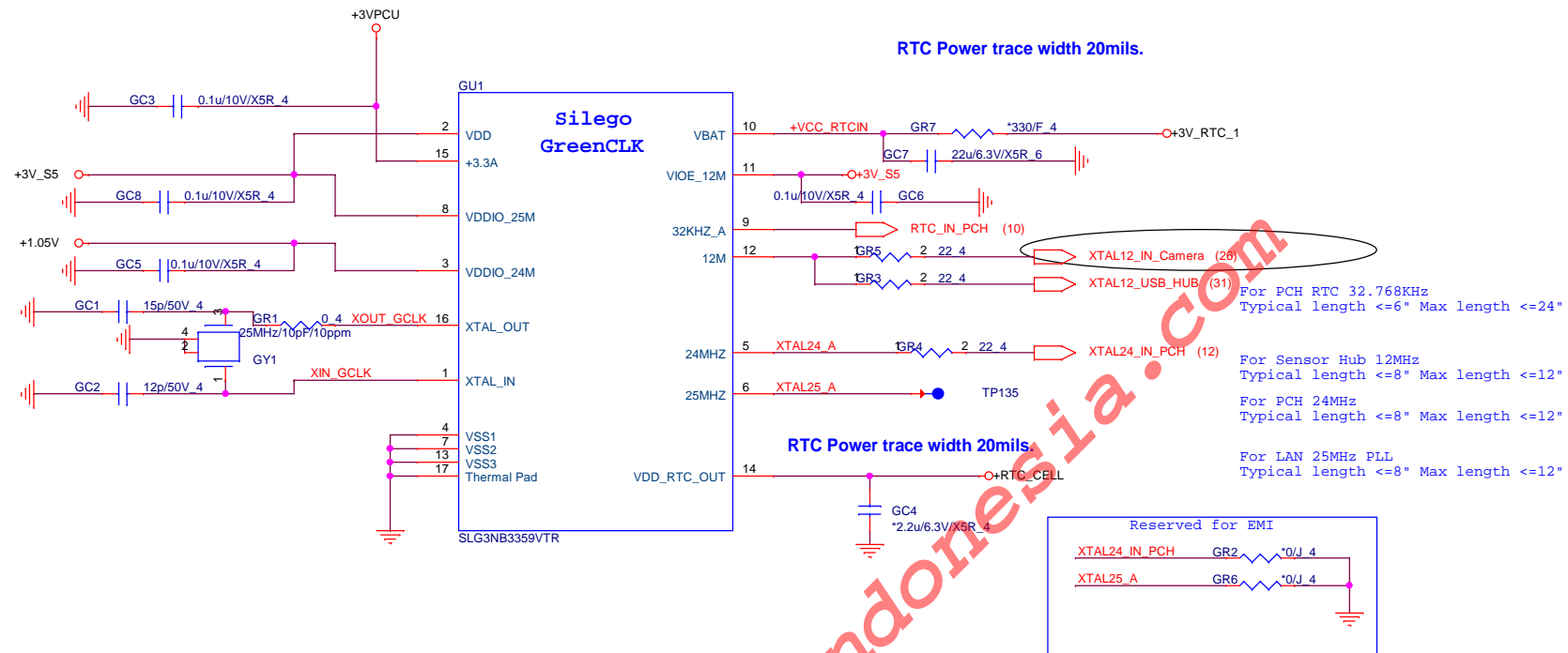
WR Address : 0xD2
RD Address : 0xD3

All surface layer delete

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.



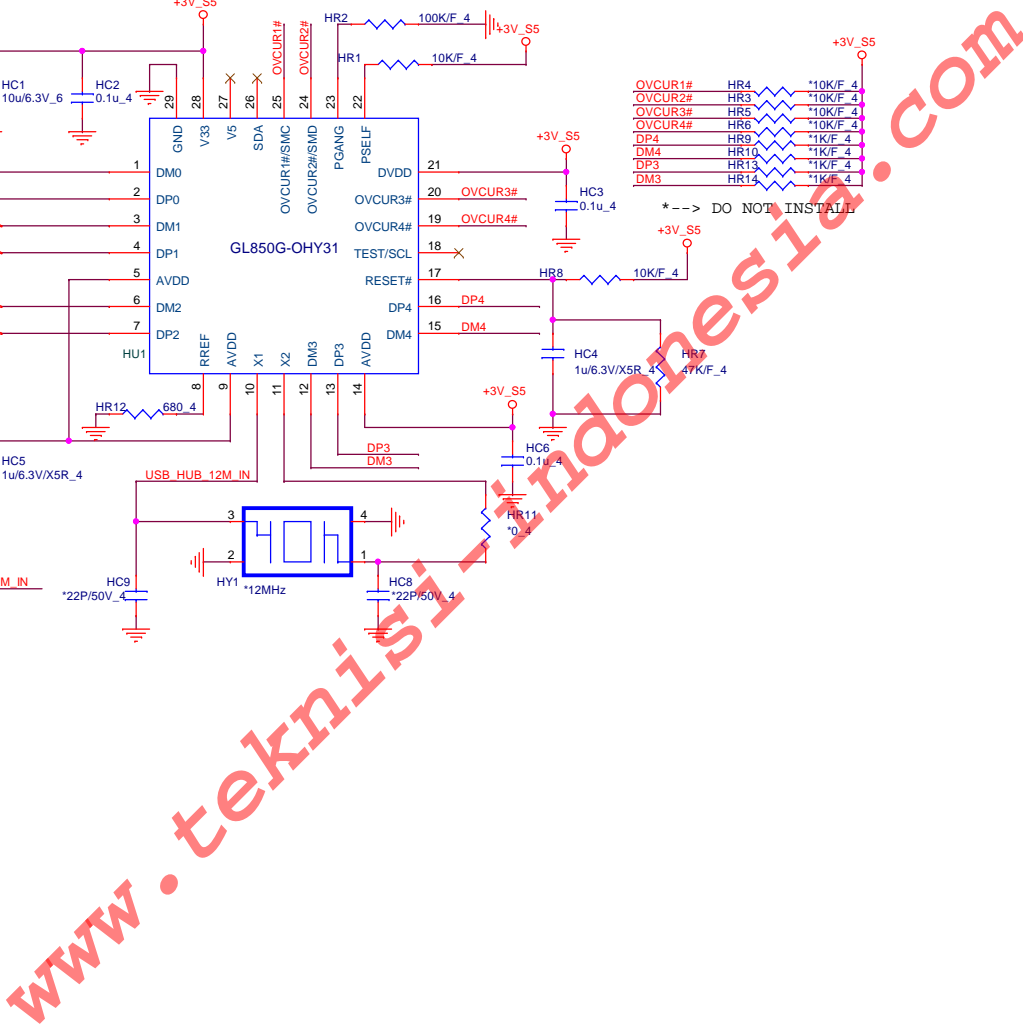
 Quanta Computer Inc. PROJECT : KR1		
Size	Document Number	Rev
	AUDIO(ALC233-CG)	1A
Date:	Monday, May 13, 2013	Sheet 29 of 44



Quanta Computer Inc.

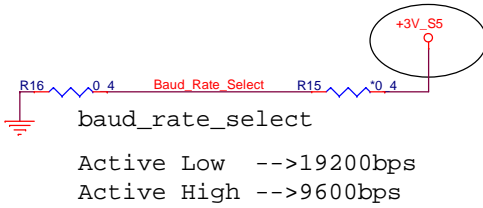
PROJECT : KR1

Size	Document Number	Rev
	Green Clork(SLG3NB3359)	1A
Date:	Monday, May 13, 2013	Sheet 30 of 44

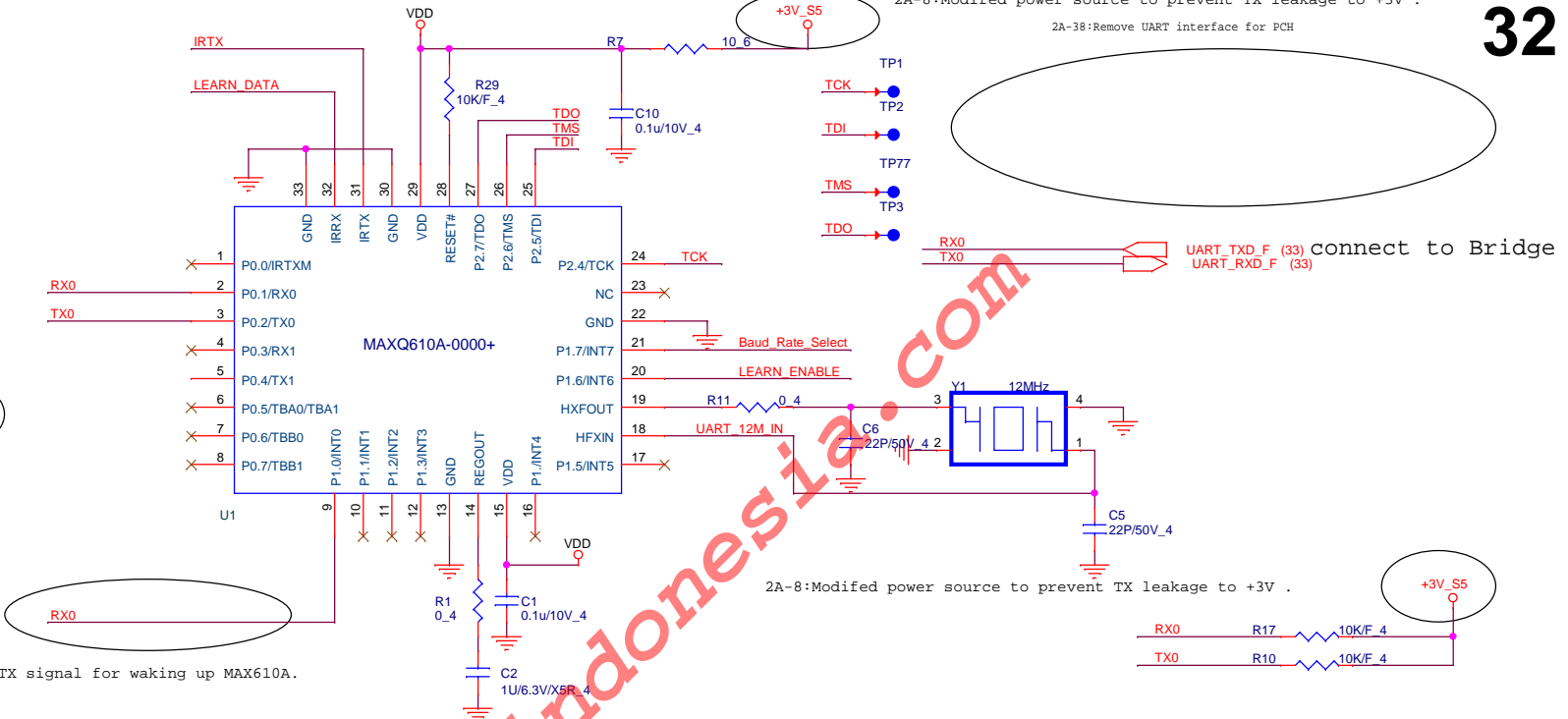


CIR MCU(MAXQ610A-0000+)

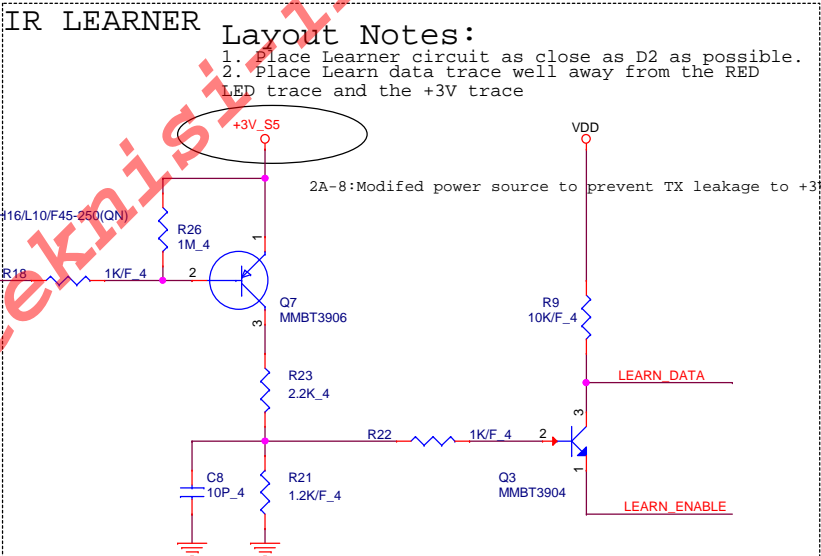
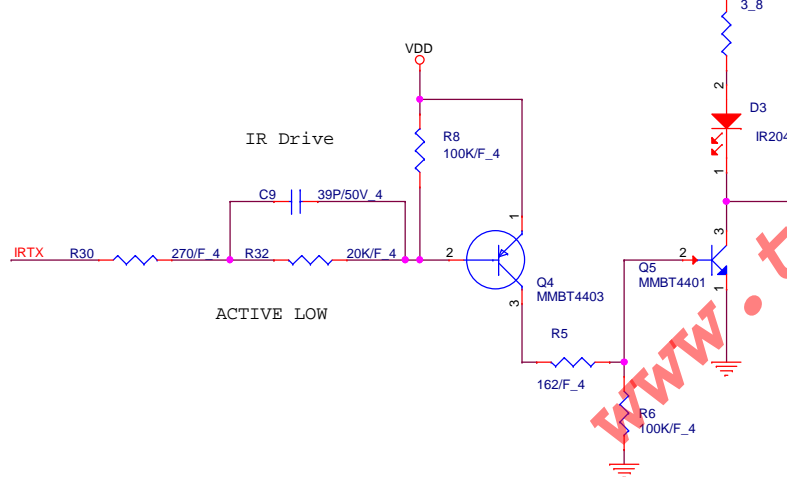
2A-8:Modified power source to prevent TX leakage to +3V .



2A-7:Connecting TX signal for waking up MAX610A.



2A-8:Modified power source to prevent TX leakage to +3V .

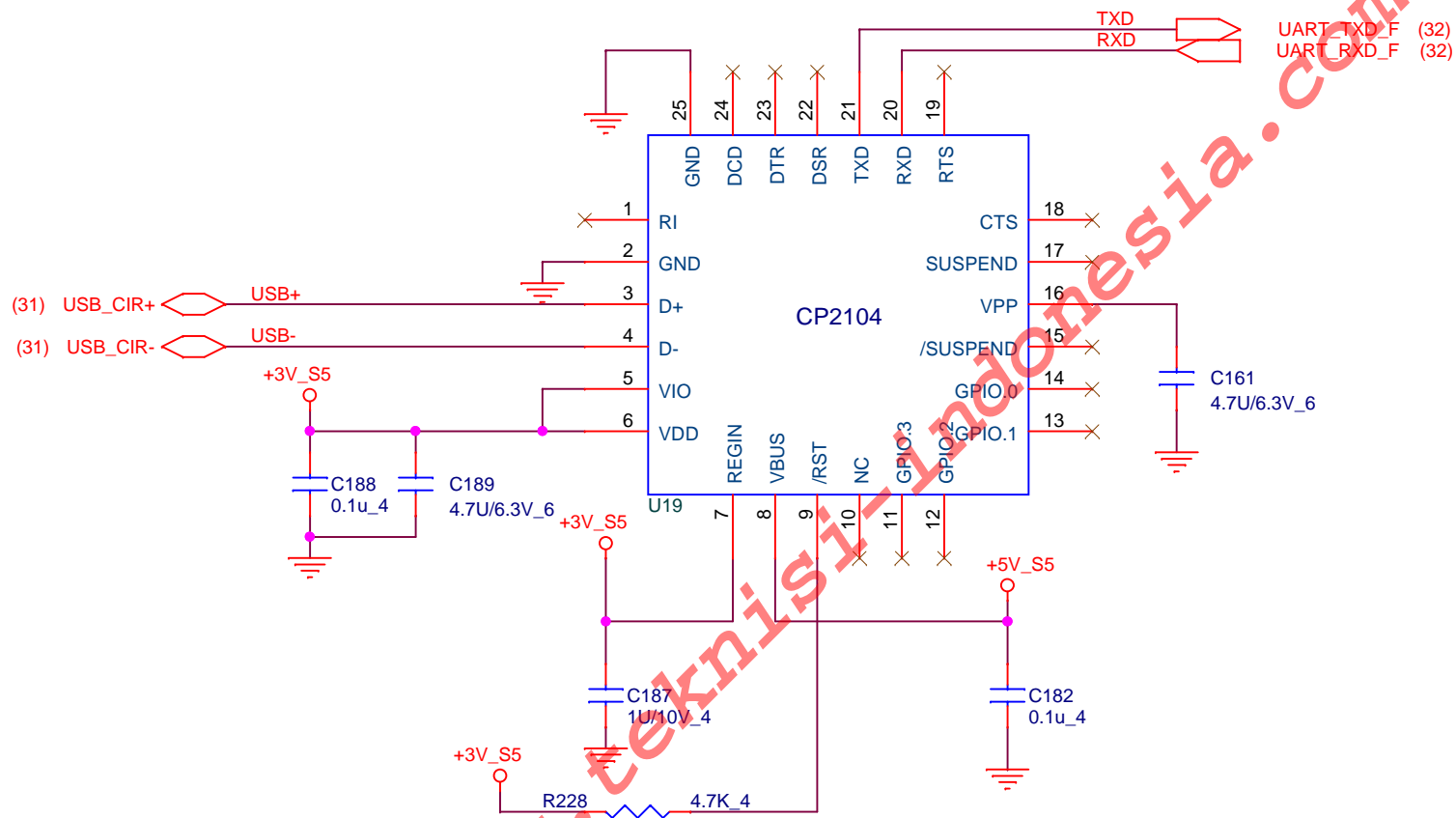


- Layout Notes:
- 1. Place Learner circuit as close as D2 as possible.
 - 2. Place Learn data trace well away from the RED LED trace and the +3V trace

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

USB TO UART(CP2104-F03-GM)

33



1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.



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PROJECT : KR1

Size	Document Number	Rev
	USB TO UART(CP2104-F03-G)	1A
Date:	Monday, May 13, 2013	Sheet 33 of 44



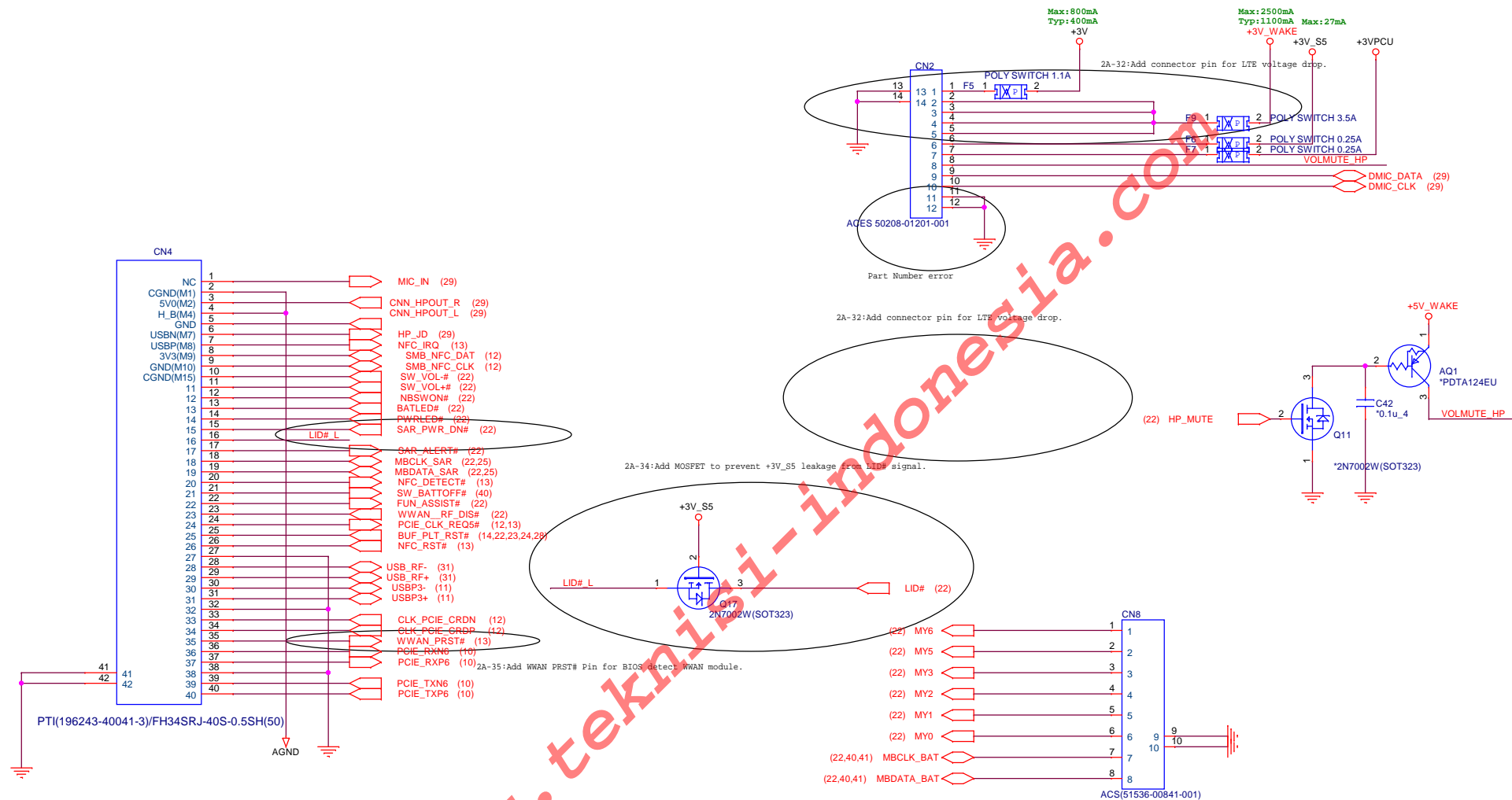
1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.



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PROJECT : KR1

Size	Document Number	Rev
	USB TO I2C(FT200XD-R)	1A
Date:	Monday, May 13, 2013	Sheet 34 of 44

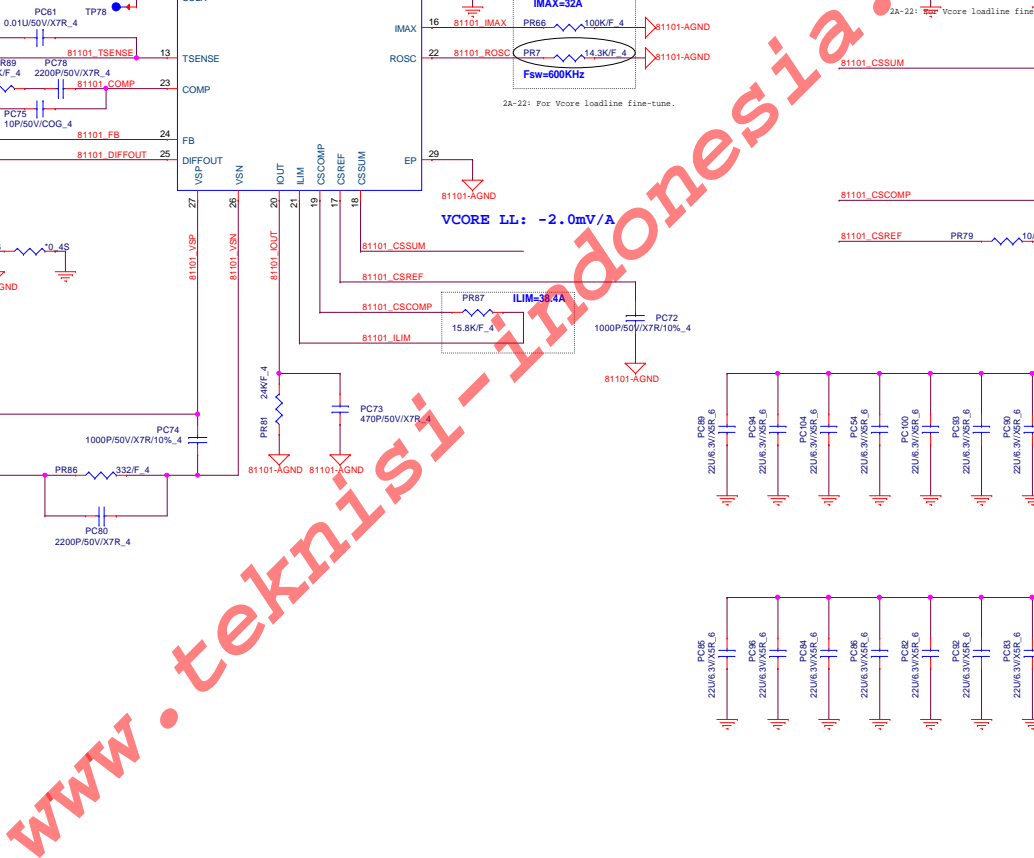


1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.



Quanta Computer Inc.
PROJECT : KR1

Size	Document Number	Rev
	Small Board	1A
Date:	Monday, May 13, 2013	Sheet 35 of 42



2A-31:Change PC33 GND to AGND for FAE suggestion

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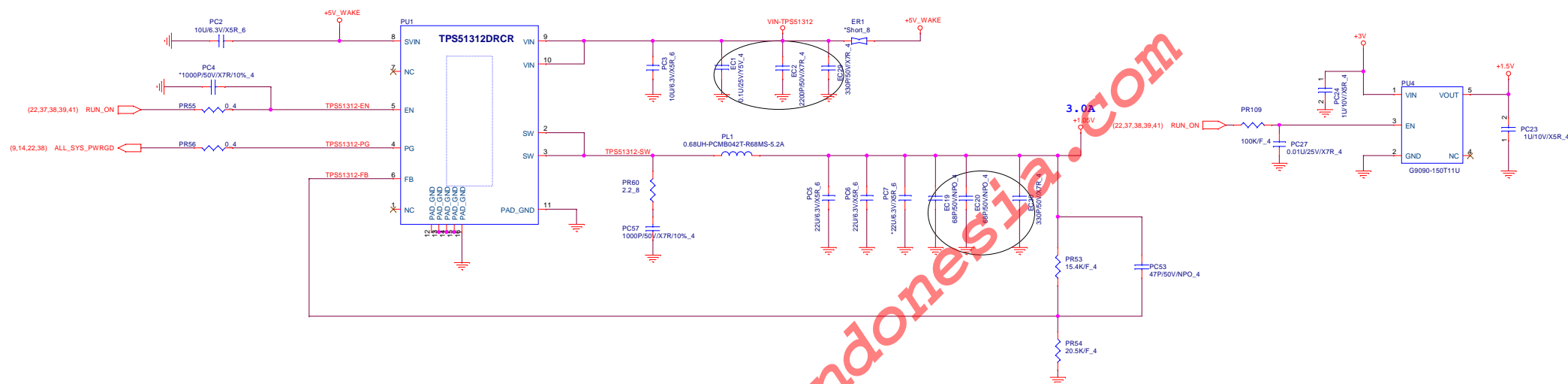
PUS

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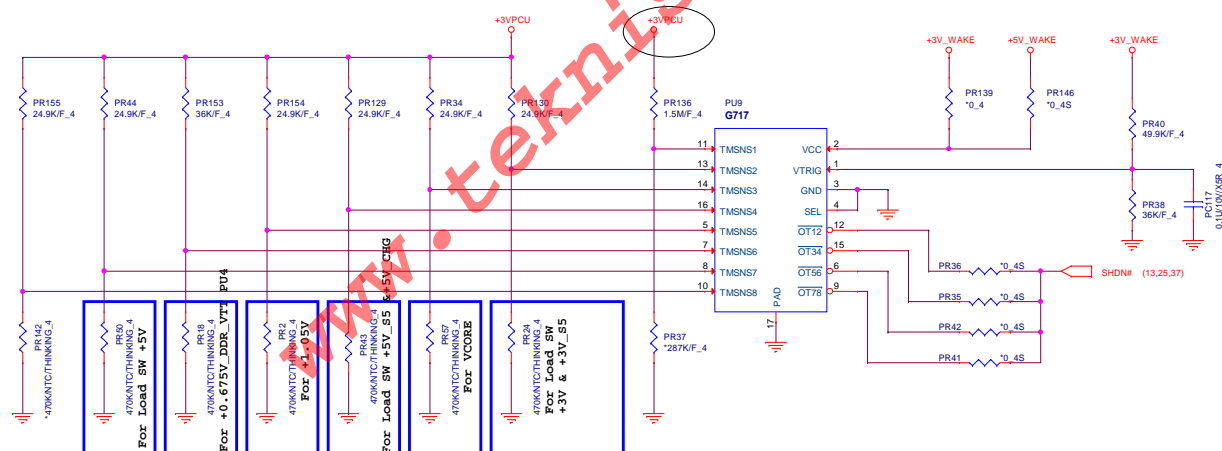
PUS

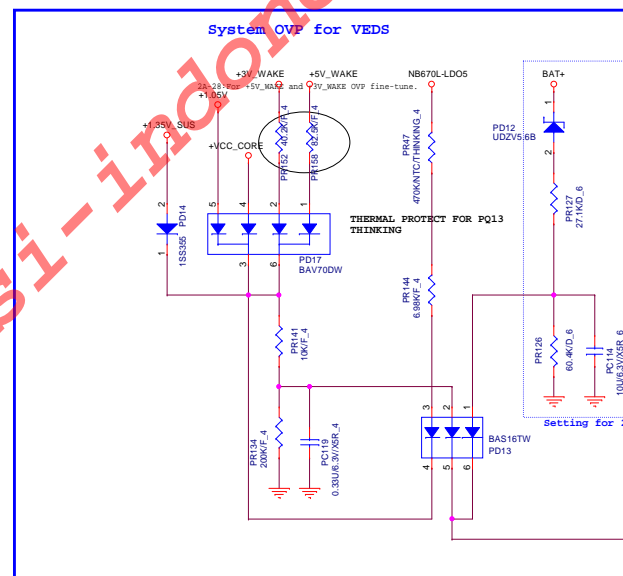
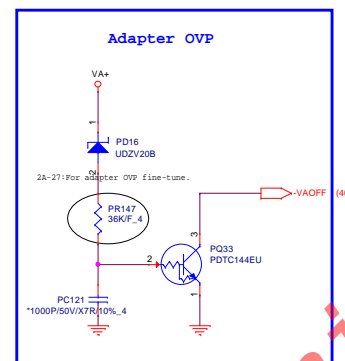
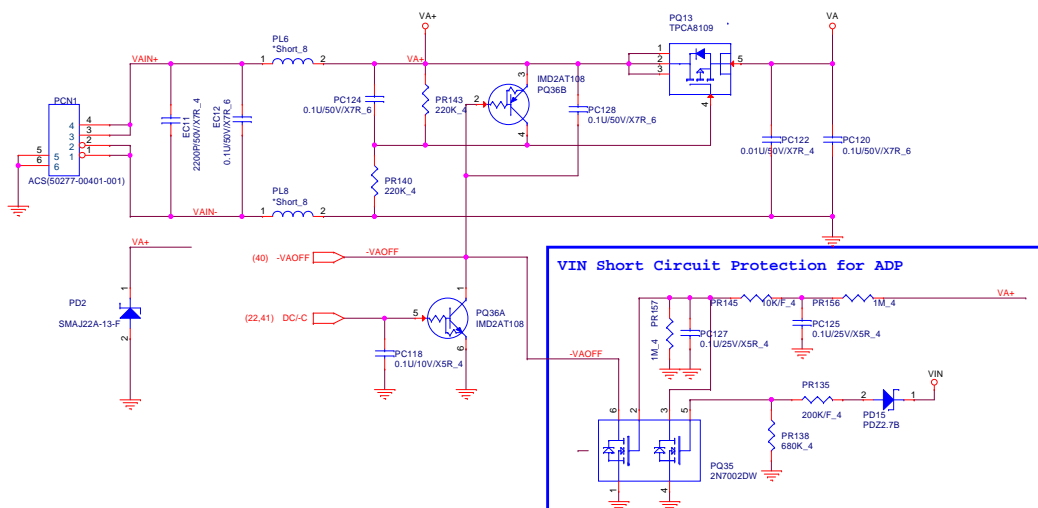
+1.05V / 3.0A



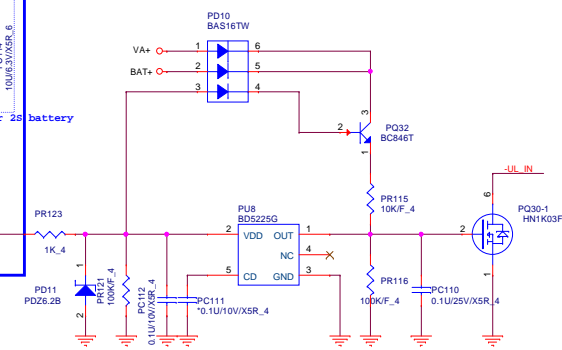
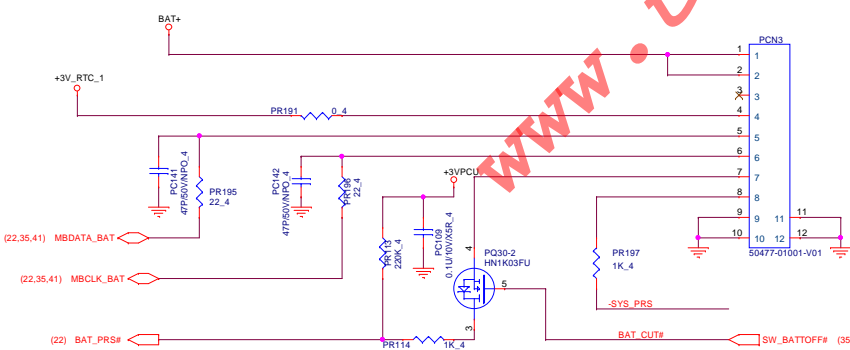
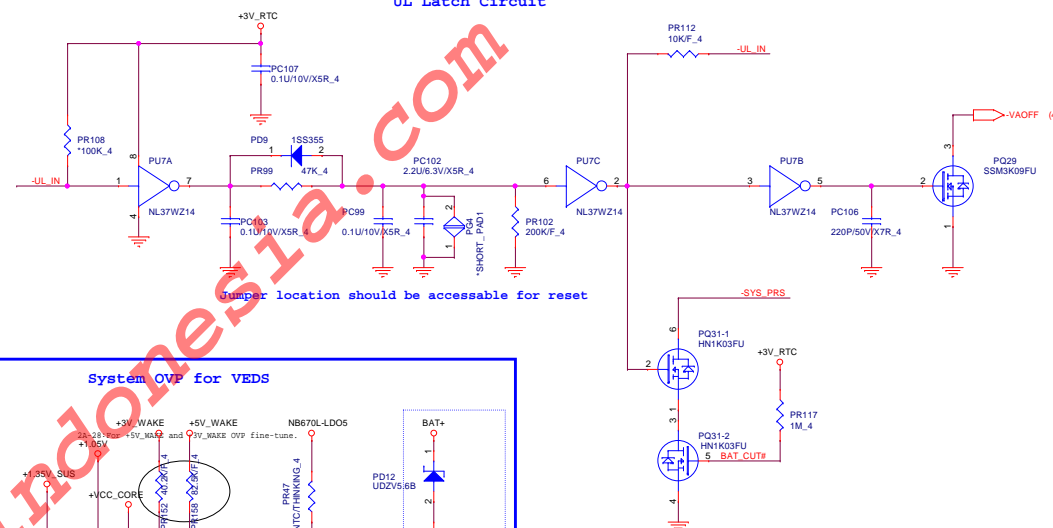
Thermal Protection

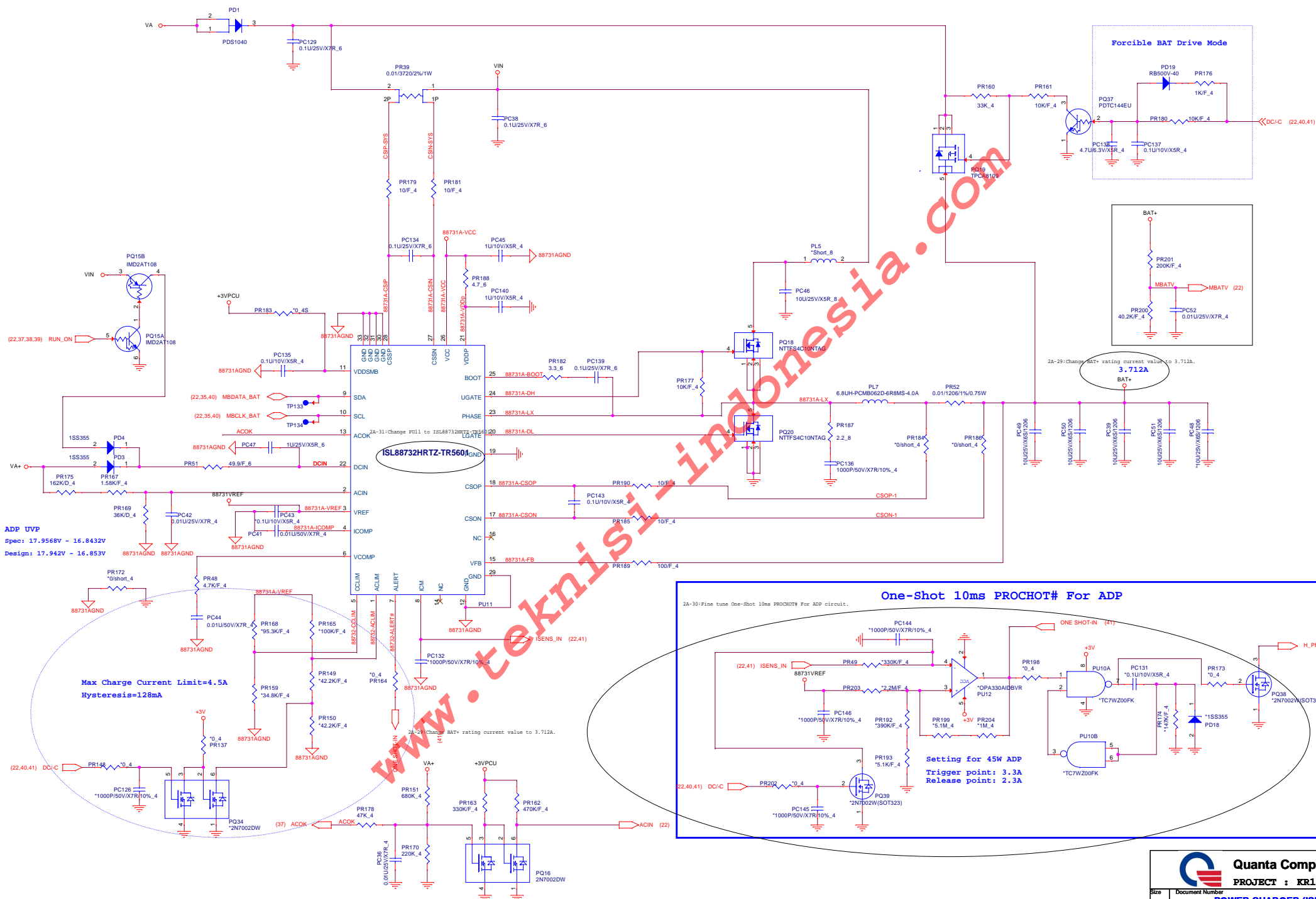
2A-26:For FU9 pin11 absolute maximum ratings 6V

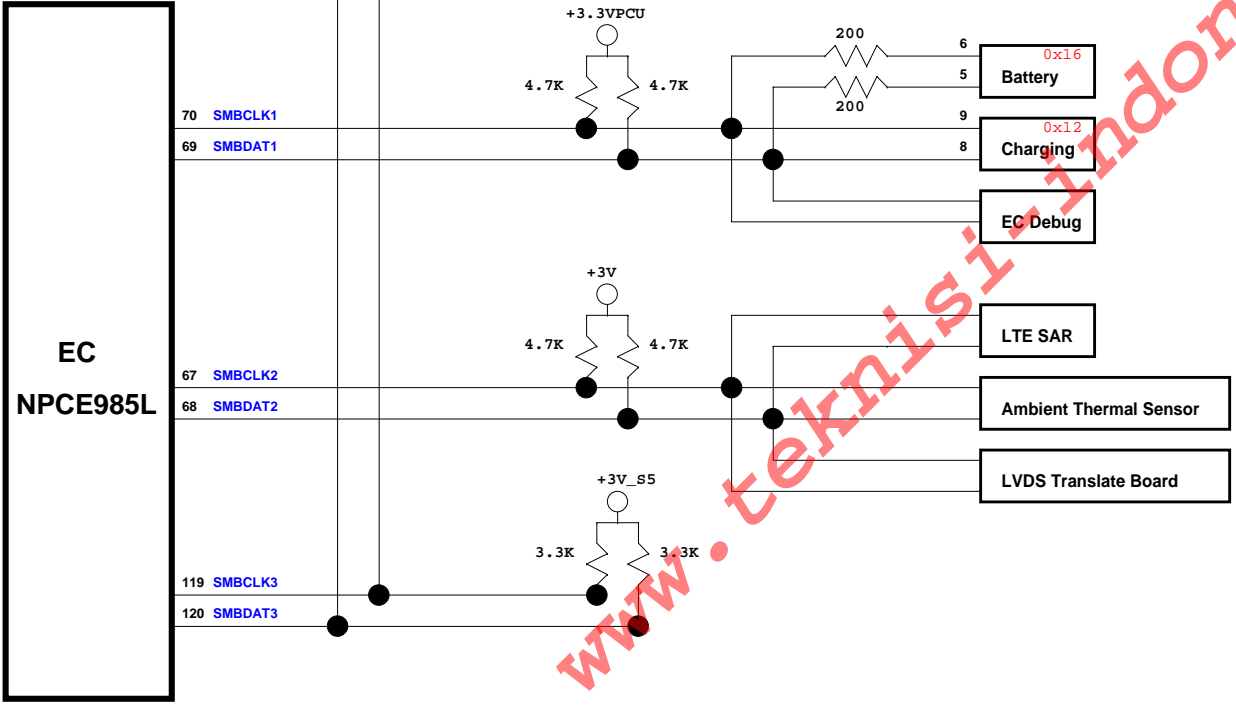
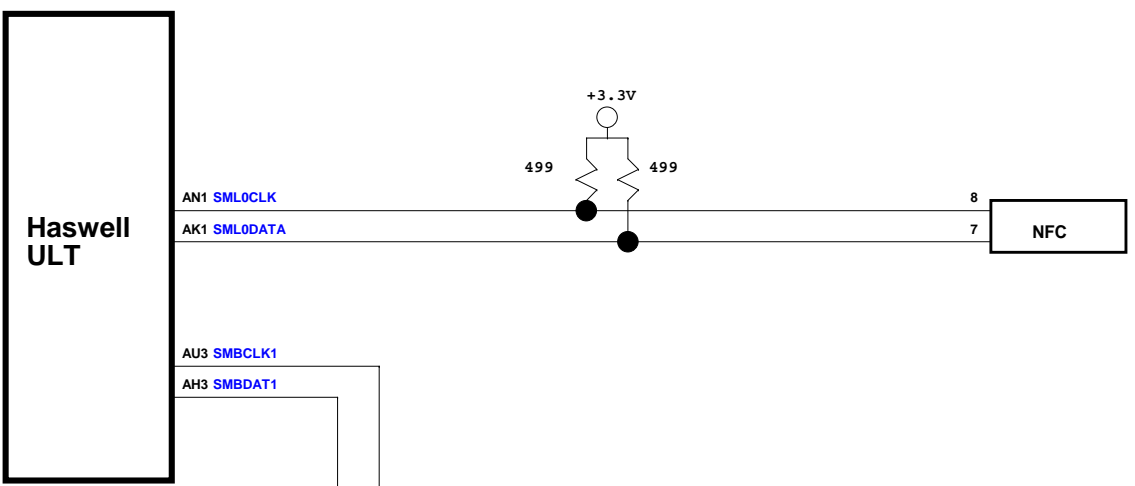




UL Latch Circuit







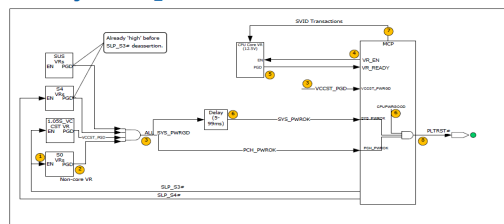
Function	IC	SMBus Address
Charge IC	ISL88731CHRTZ	0X12
Battery	Battery	0X16
NFC		

1.Level 1 Environment-related Substances Should Never be Used.
2.Recycled Resin and Coated Wire should be procured from Green Partners.

Power	Voltage	S0	S3	DS3	S4 (/W RTC Wake up)	S4 (/WO RTC Wake up)	S4 (/WO CHANGE)	S4 (/W CHANGE)	S5 (/WO CHANGE)	S5 (/W CHANGE)	Ctl Signal
+3VPCU	3.3V	V	V	V	V	V	V	V	V	V	Adapter/BAT in
+3.3V_DSW	3.3V	V	V	V	V	V	V	V	V	V	DEEP_EC_EN
+3V_WAKE	3.3V	V	V	V	V			V		V	EC_WAKE_ON
+5V_WAKE	5V	V	V	V	V			V		V	EC_WAKE_ON
+5V_S5	5V	V	V		V						S5_ON
+3V_S5	3.3V	V	V		V						S5_ON
+1.35V_SUS	1.35V	V	V	V							SUS_ON
+3V	3.3V	V									RUN_ON
+5V	5V	V									RUN_ON
+0.675V_DDR_VTT	0.675V	V									RUN_ON
+1.05V	1.05V	V									RUN_ON
+1.5V	1.5V	V									RUN_ON
+VCC_CORE	By VID	V									RUN_ON

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Figure 2-4. Flow Diagram for SYS_PWROK Generation – ULT Platform



AC IN --> EC LOAD CODE

